Nano-electronic Stochastic Logic Gates - Memory Devices - Sensors and Energy Harvester

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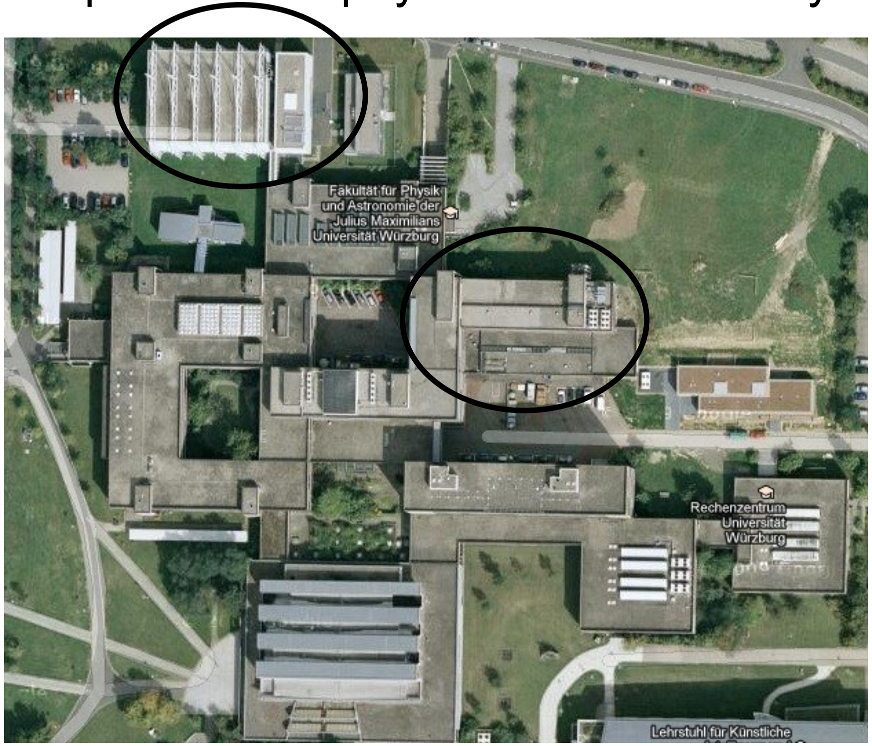
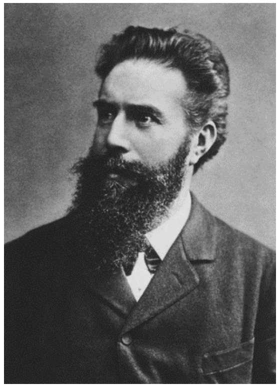
Department of physics and astronomy: An overview

Department of physics and astronomy



Source: google.de/maps

8 experimental physics chairs
5 theoretical physics chairs
+ several experimental and theoretical work groups



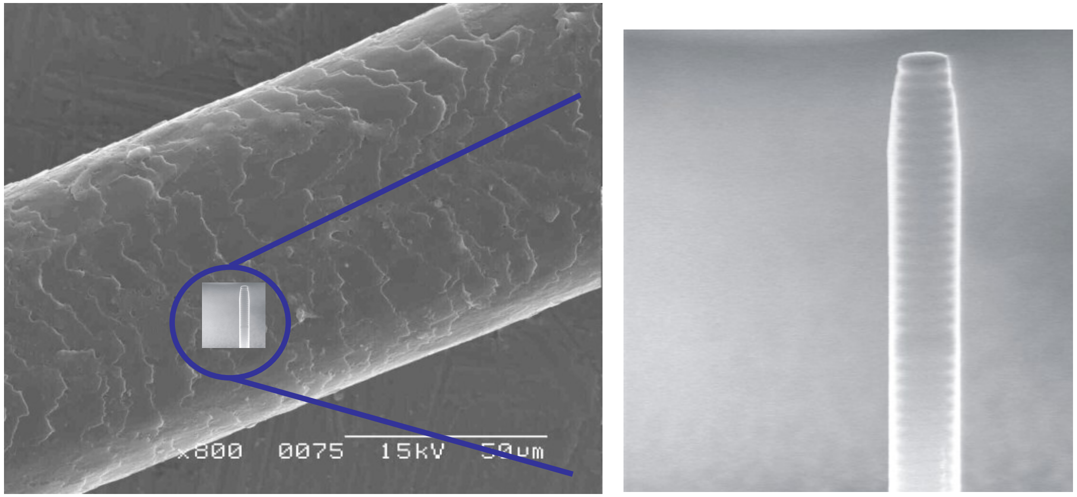
Wilhelm C. Röntgen
First Nobel Prize 1901
(X-rays)

Klaus von Klitzing
Nobel Prize 1985
(Quantum Hall effect)

Other nobel laureates with a Würzburg history:

- Wilhelm Wien, Johannes Stark, Svante Arrhenius, Ferdinand Braun, Max von Laue, “Werner Heisenberg”

Quantum electrodynamics



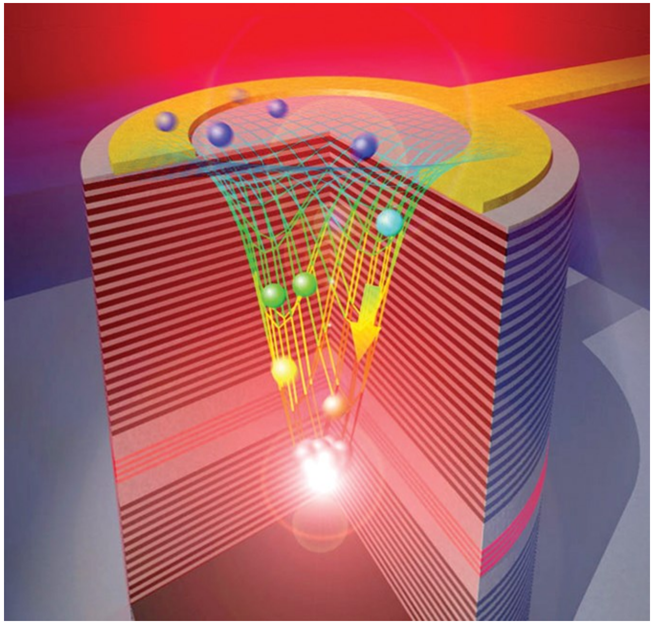
J.P. Reithmaier et al., „Strong coupling in a single quantum dot–semiconductor microcavity system“, *Nature* **432**, 197-200 (11 November 2004).

Mars Exploration Rover Mission


Picture: Courtesy of NASA/JPL - Caltech

http://www.nanoplus.com/index.php?option=com_content&view=article&id=78

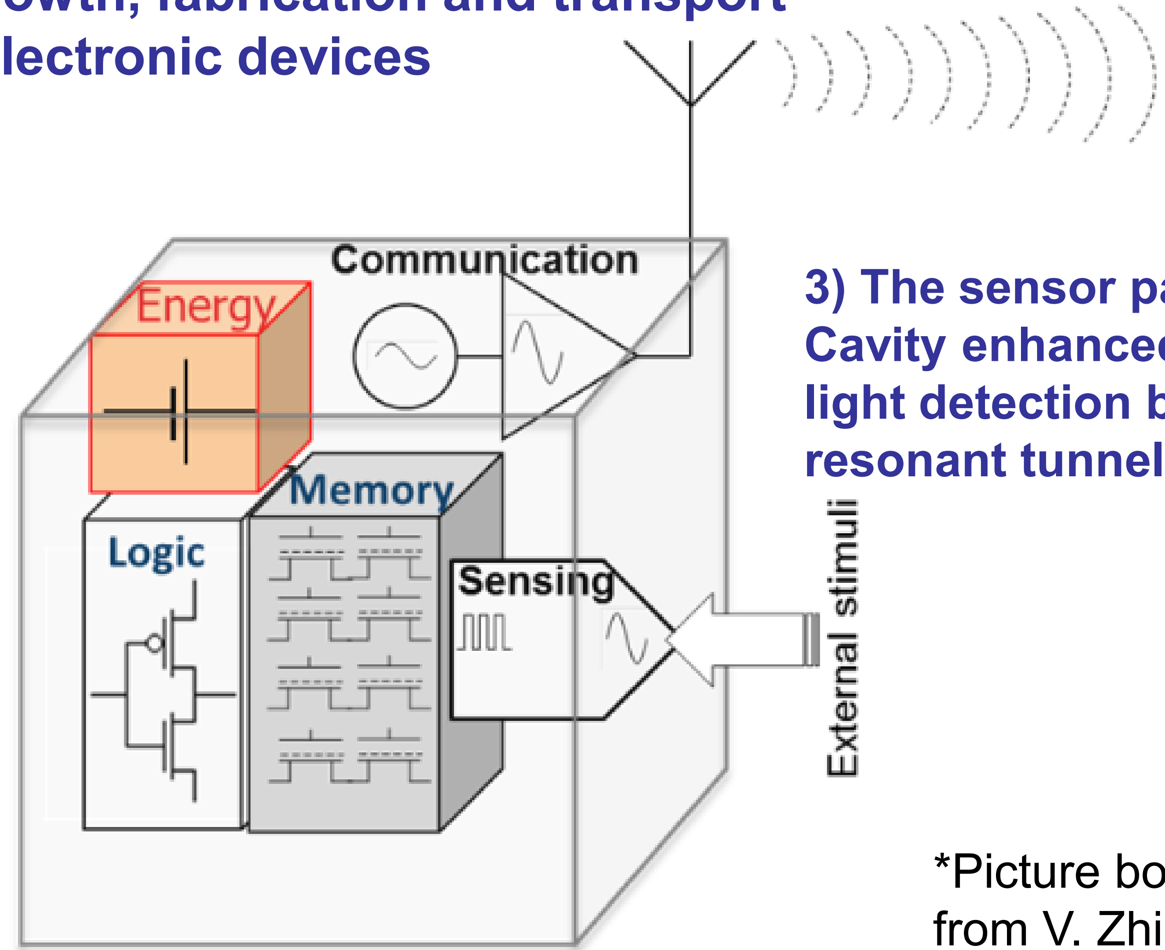
Polariton laser



"An electrically pumped polariton laser"
C. Schneider et al., Nature 497, 348–352 (2013).

Outline

0) The intro part: Growth, fabrication and transport properties of nanoelectronic devices



4) The energy harvester part: Voltage fluctuation to current conversion

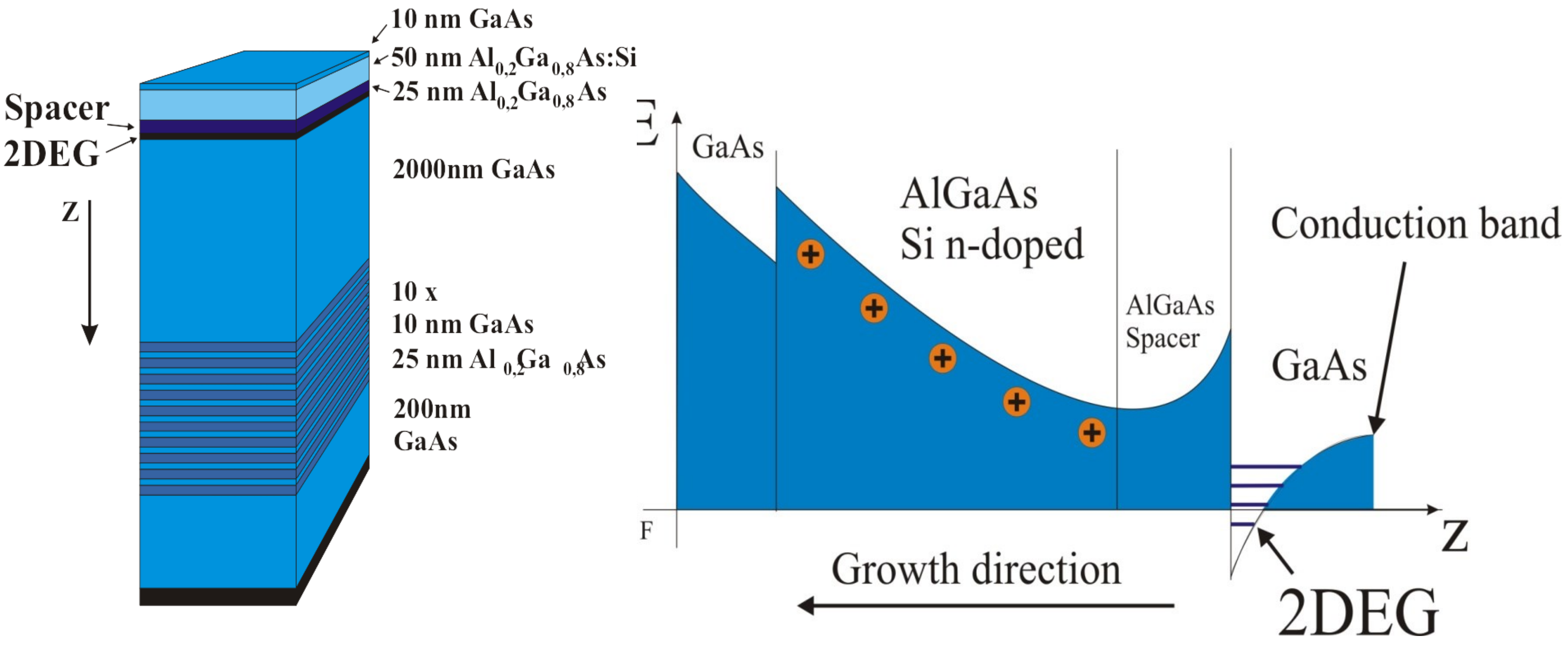
3) The sensor part: Cavity enhanced light detection by resonant tunneling

1) The logic gate part: Stochastic universal logic gates

2) The memory part: Quantum dot floating gate transistor

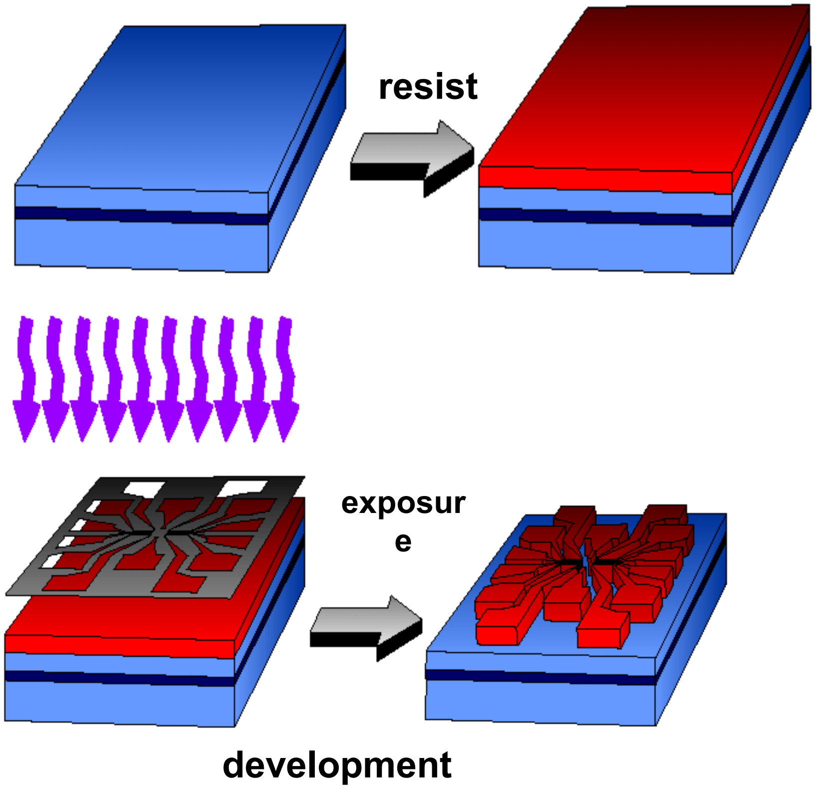
*Picture borrowed from V. Zhirnov‘s talk

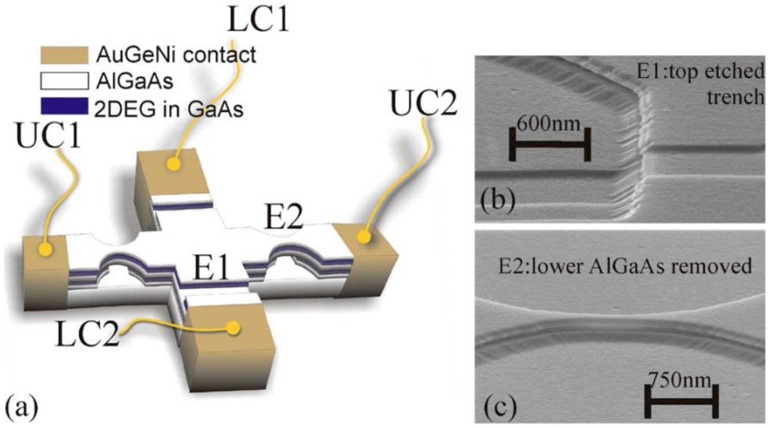
Growth of high mobility two dimensional electron gases based on AlGaAs/GaAs

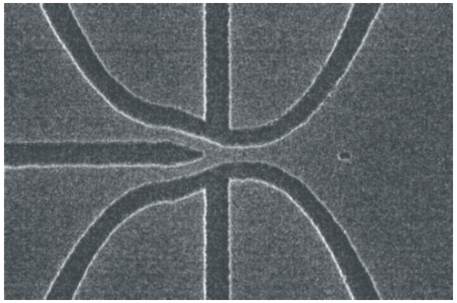


- Modulation doped GaAs/AlGaAs heterostructure.
- Grown by molecular beam epitaxy.
- High mobility $\mu = 1.1*10^6$ cm^2/Vs and charge density $n = 3.7*10^{11}$cm^{-2}.

Fabrication of electron waveguides and other nanoelectronic devices – Top down



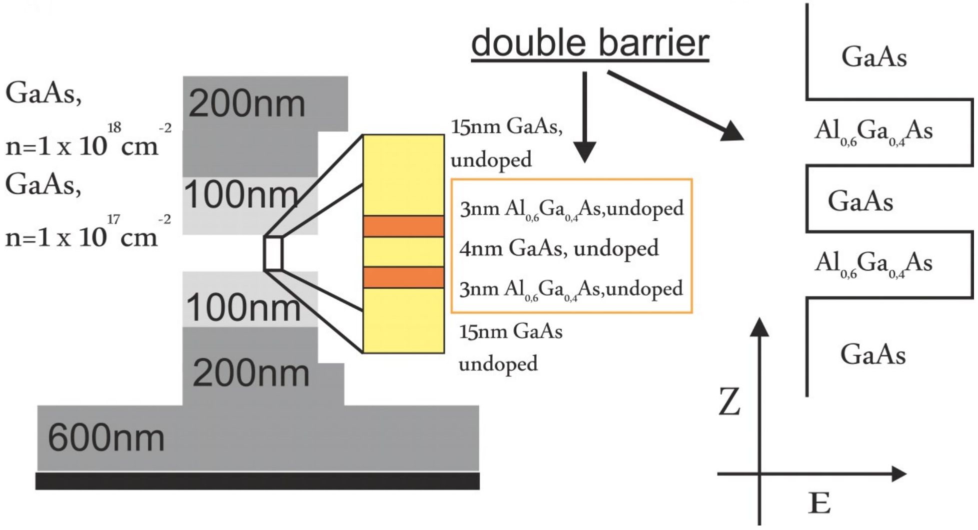


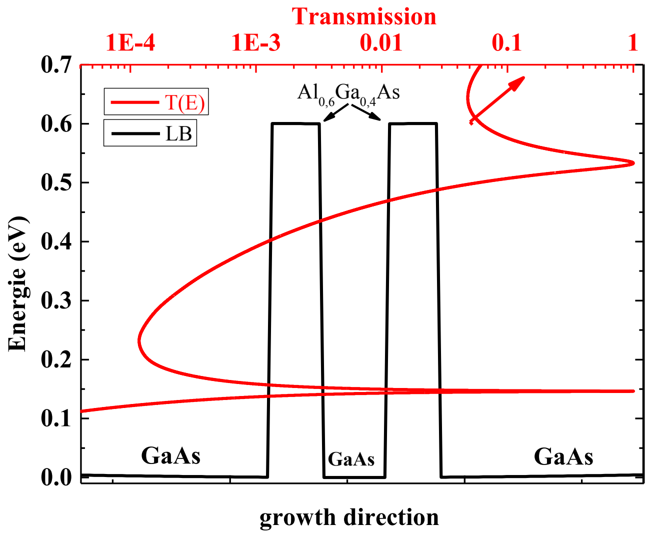


- Electron beam or optical lithography.
- Wet or dry chemical etching (e.g. ECR-RIE).

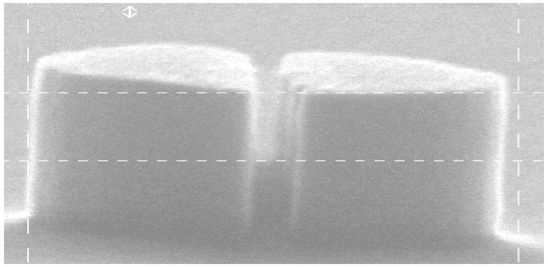
Fabrication and working principle of resonant tunneling diodes

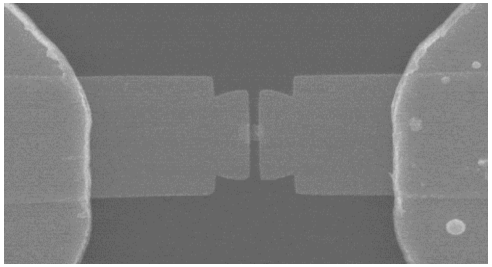
GaAs based RTDs with AlGaAs barriers.

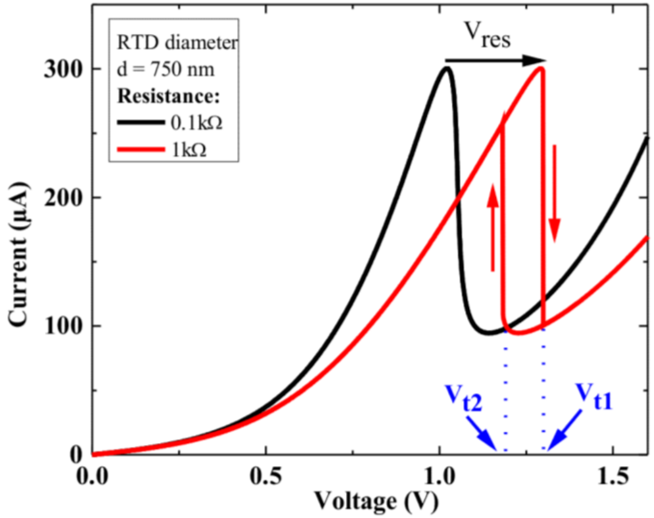




Trench etched RTD

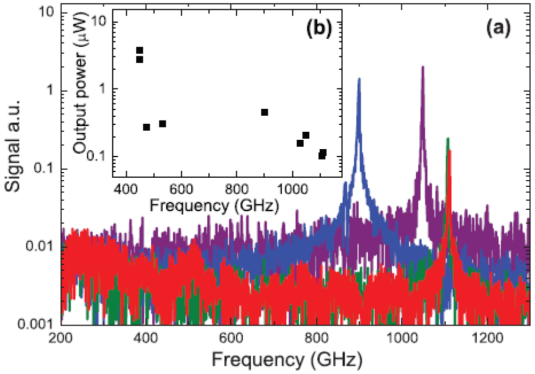






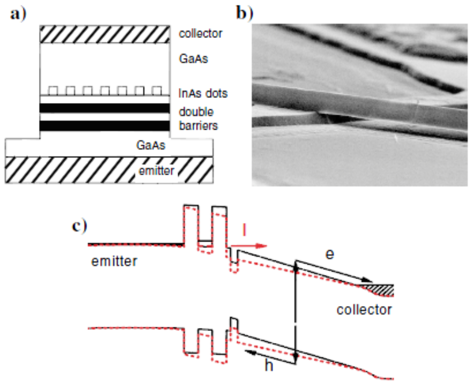
Applications of electron waveguide devices and resonant tunneling diodes

Oscillator



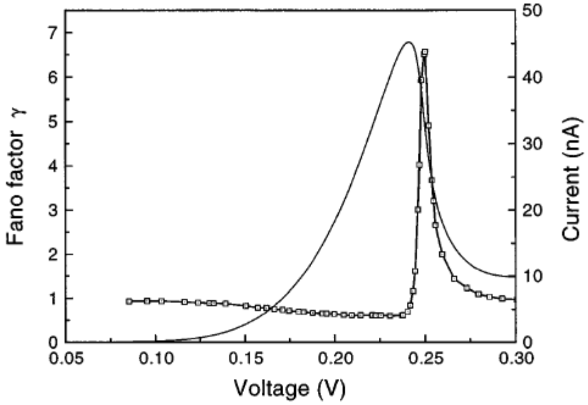
Feiginov et al., Appl. Phys. Lett. 99, 233506 (2011).

Photosensor



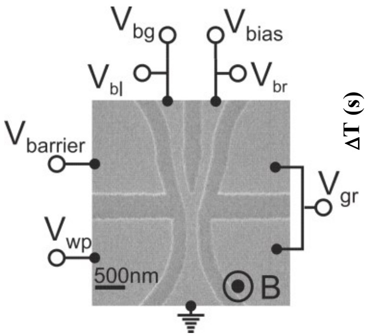
J. C. Blakesley, et al., PRL **94,** 067401 (2005).

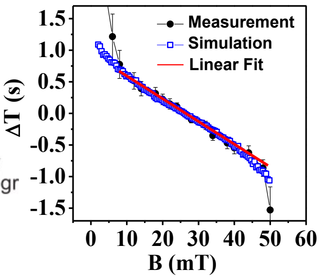
Noise correlation



G. Iannaccone et al., PRL 80, 1054-1057 (1998).

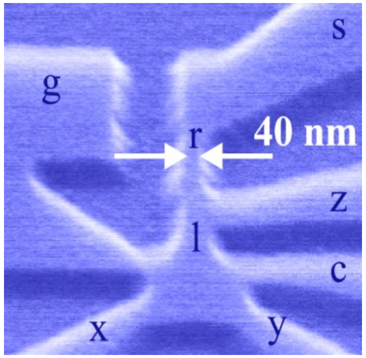
Noise activated nonlinear dynamical sensor





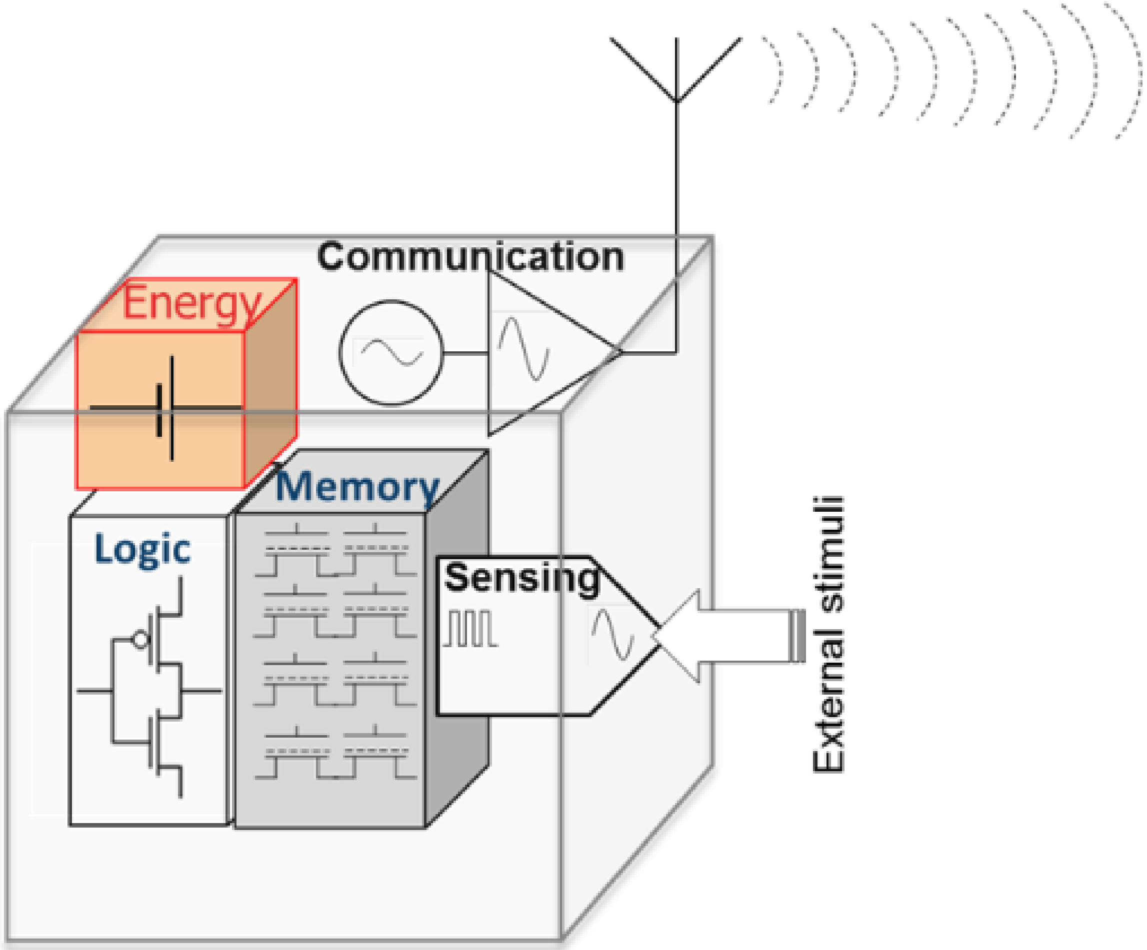
F. Hartmann et al, Appl. Phys. Lett. **96**, 082108 (2010).

Half and full adder



B. Lau, D. Hartmann, L. Worschech and A. Forchel, IEEE Transactions on Electron Devices 53, 1107 (2006)

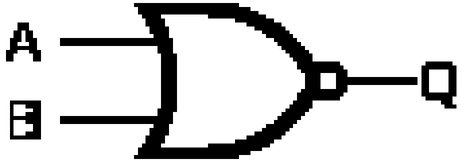
Outline



1) The logic gate part: Stochastic universal logic gates

Universal logic gates – NOR and NAND gate

NOR gate:

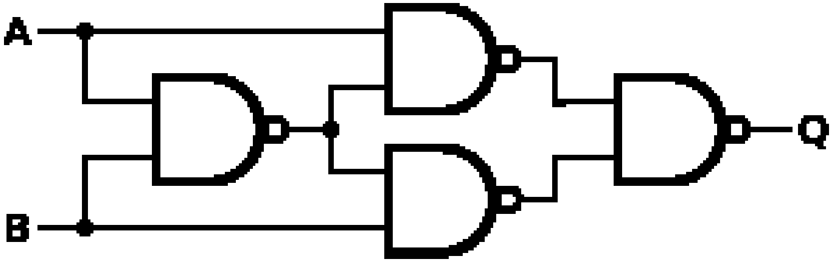


Truth table:

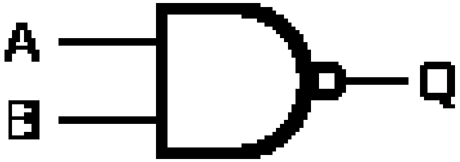
A	B	Q
0	0	1
1	0	0
0	1	0
1	1	0

XOR gate (binary sum):

A	B	Q
0	0	0
1	0	1
0	1	1
1	1	0



NAND gate:



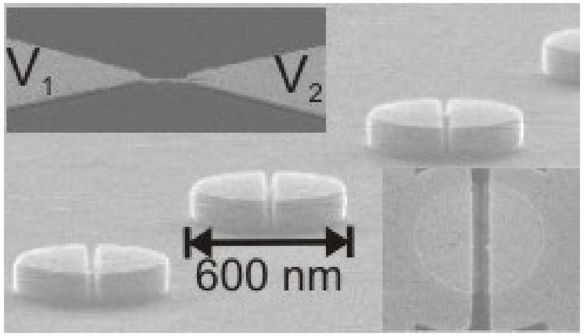
Truth table:

A	B	Q
0	0	1
1	0	1
0	1	1
1	1	0

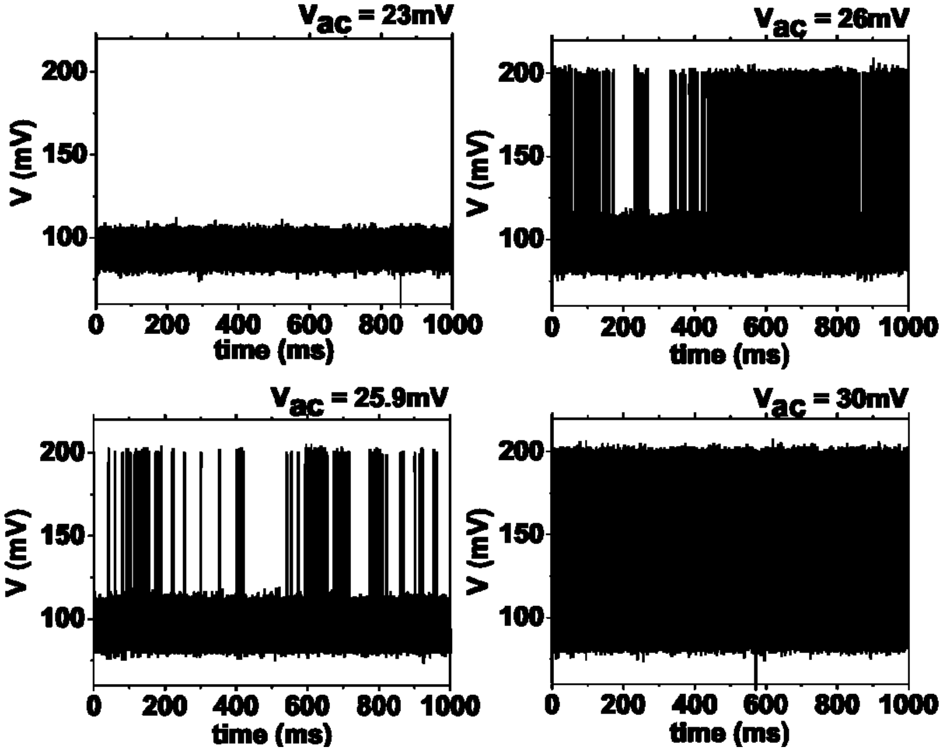
Universal logic gate:

- Any logic gate can be made from a combination of NAND or NOR gates.

Reconfigurable logic universal gates: Noise induced firing rates in RTDs

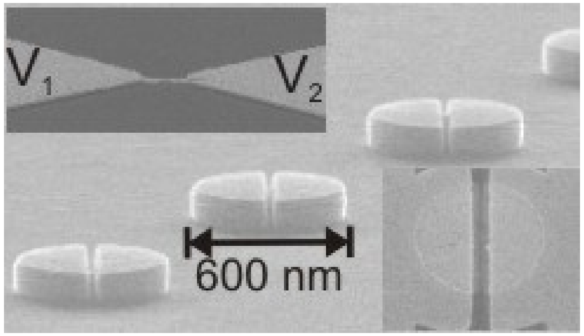


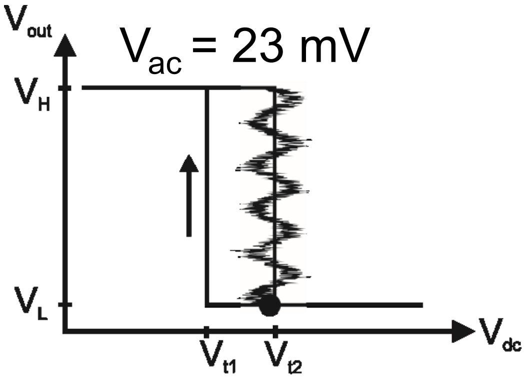
- ❒ Electron microscopy images of a trench etched RTD with diameter d = 600 nm
- ❒ Branches serve as logical inputs

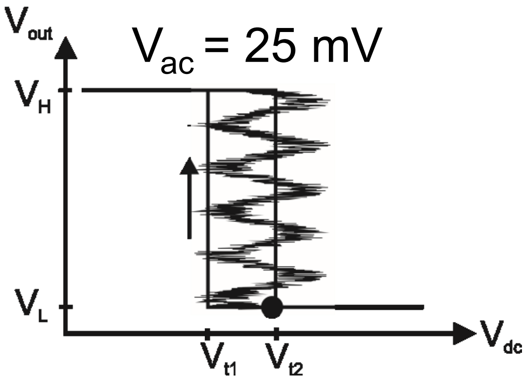


- ❒ Noise induced signal trains
- ❒ Mean value is efficiently controlled by input signals
- ❒ Can be integrated to arrays
- ❒ No classical kT limit of transconductance

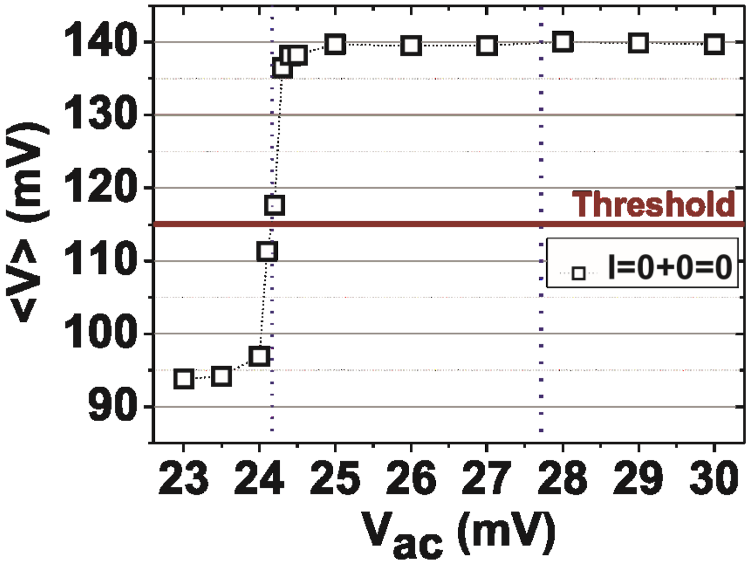
Reconfigurable logic universal gates: NOR and NAND configurations

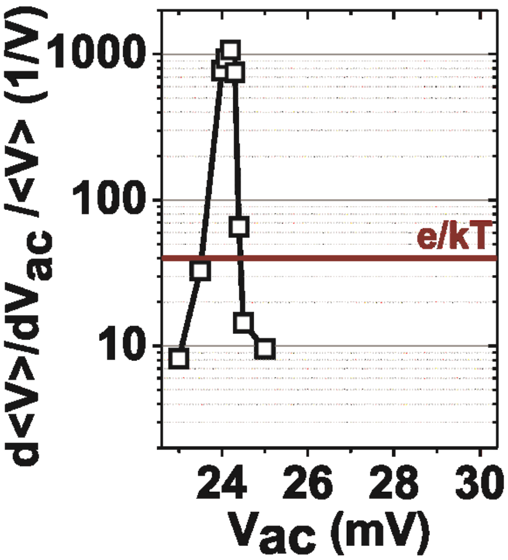




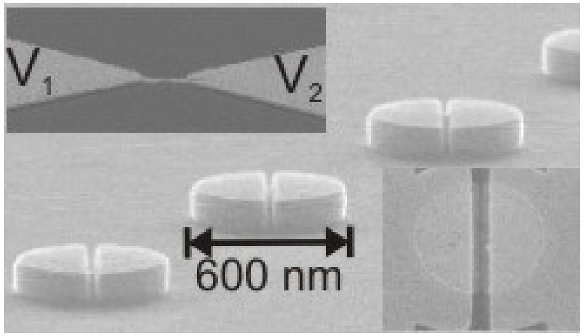


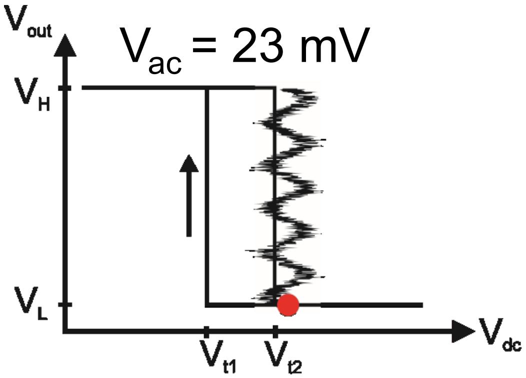
Switching voltages: $V_1 = V_2 = 0$mV

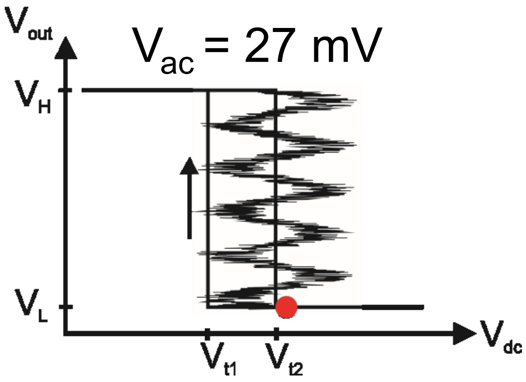




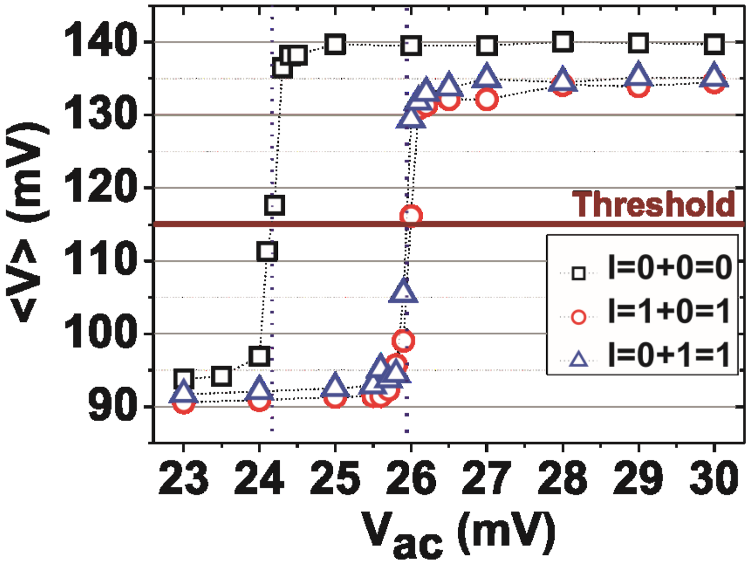
Reconfigurable logic universal gates: NOR and NAND configurations

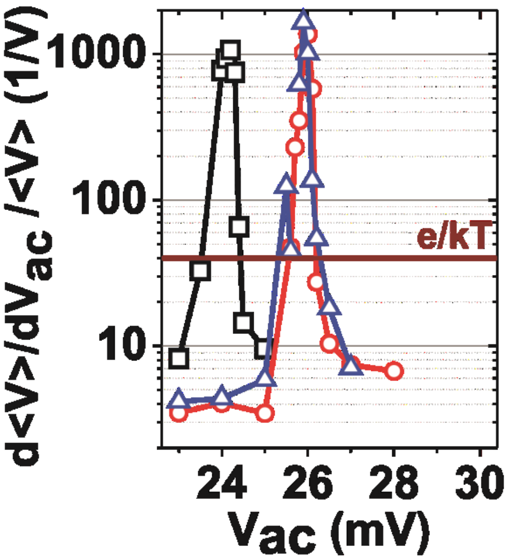




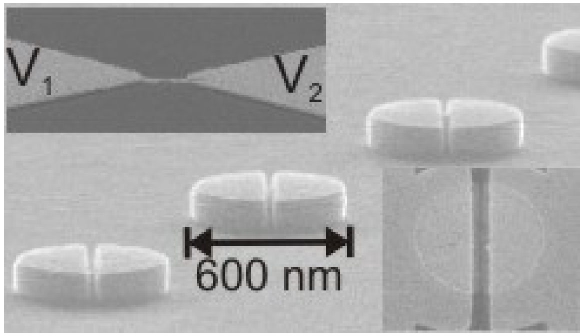


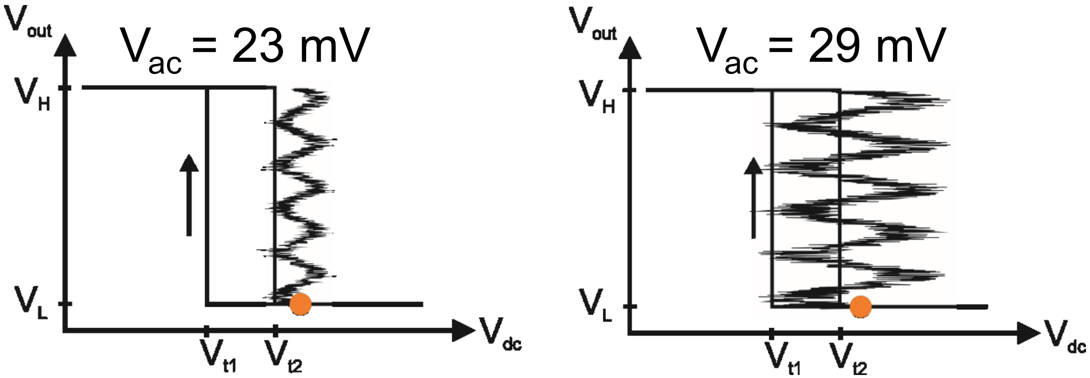
Switching voltages: V_1 = 0, 2 mV V_2 = 2, 0 mV



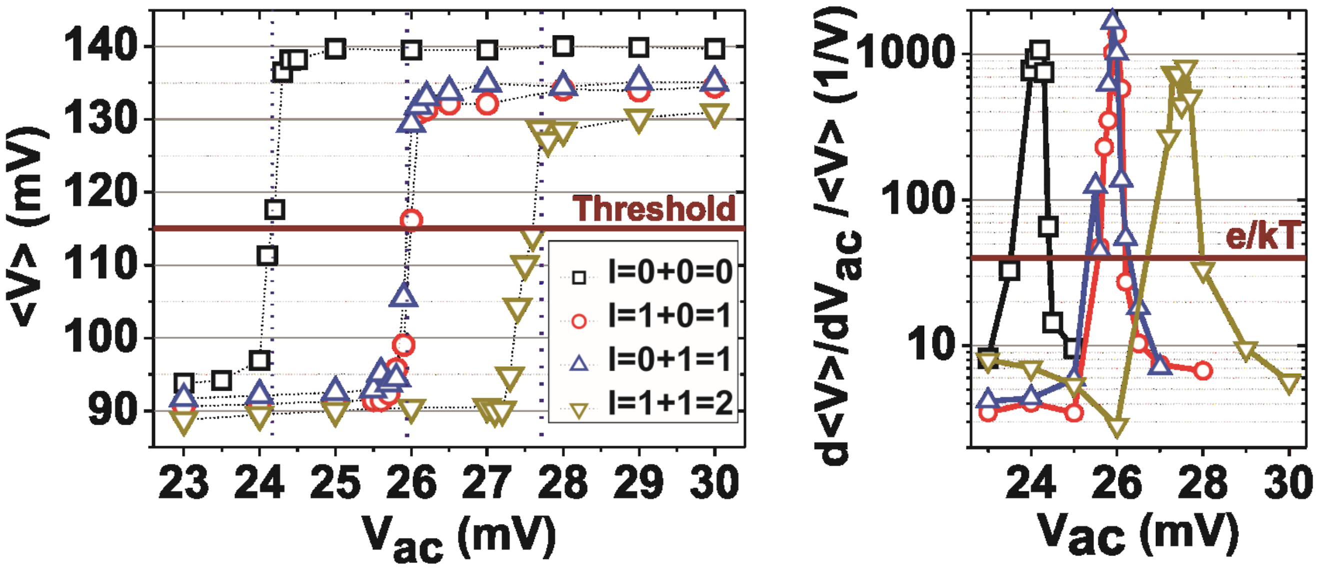


Reconfigurable logic universal gates: NOR and NAND configurations

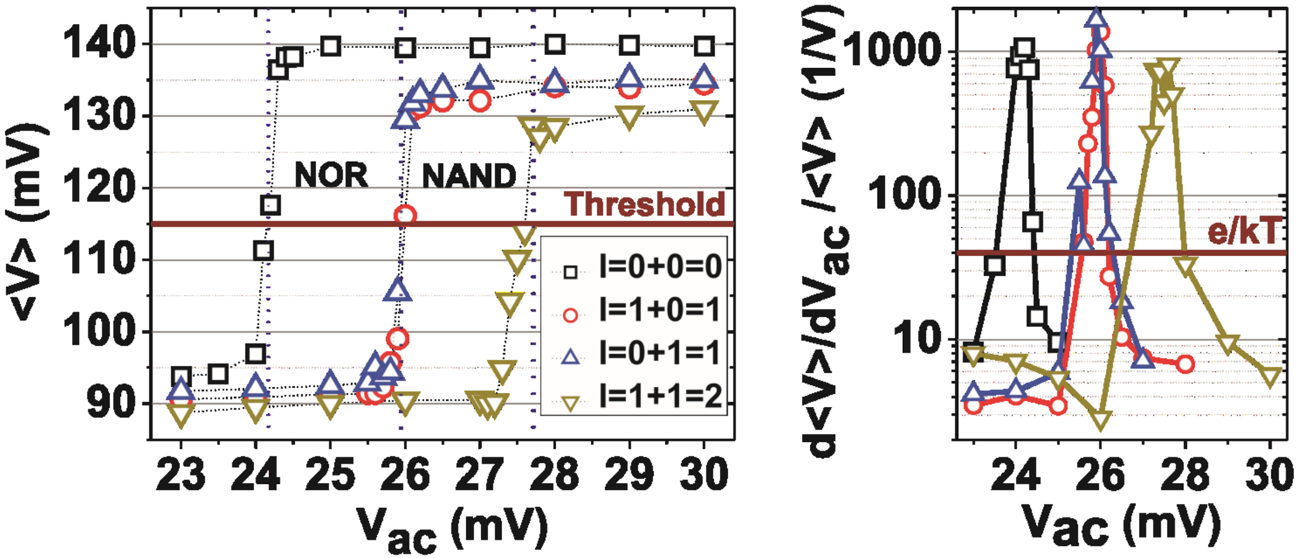




Switching voltages: $V_1 = V_2 = 2$ mV



Reconfigurable logic universal gates: NOR and NAND configurations & truth tables



NOR

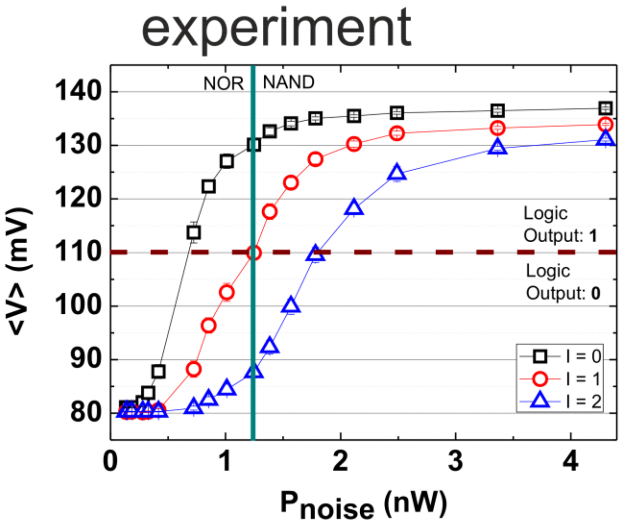
0 0 | 1
1 0 | 0
0 1 | 0
1 1 | 0

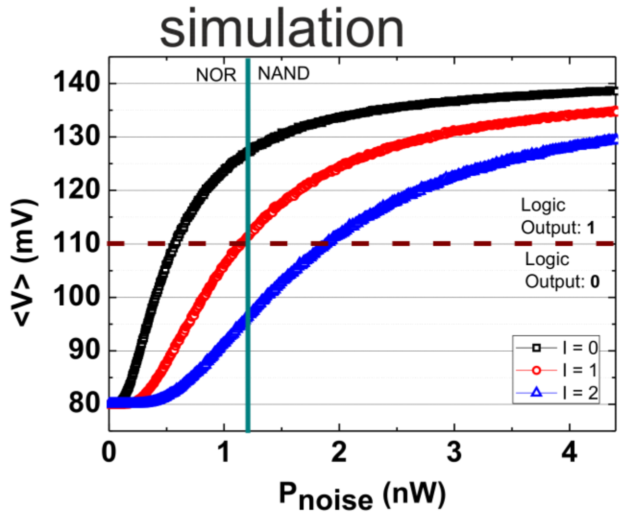
NAND

0 0 | 1
1 0 | 1
0 1 | 1
1 1 | 0

- Switch from NOR to NAND for ΔV_{ac} < 1 mV with a logic input voltage 2 mV

Reconfigurable logic universal gates: Logic stochastic resonance





Previous:

- Universal logic gate switching controlled the amplitude of the periodic forcing.

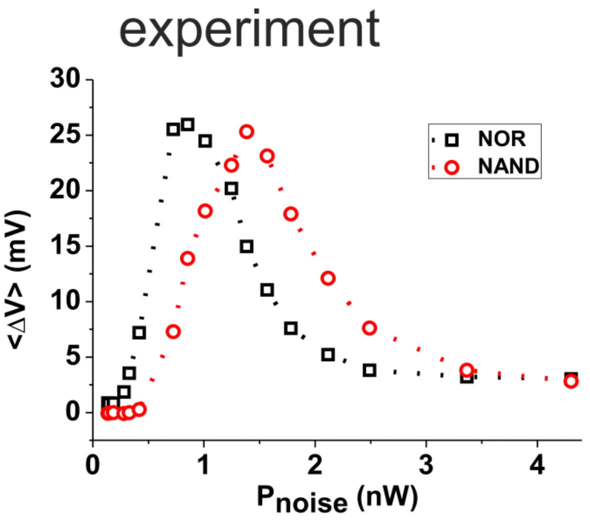
Now:

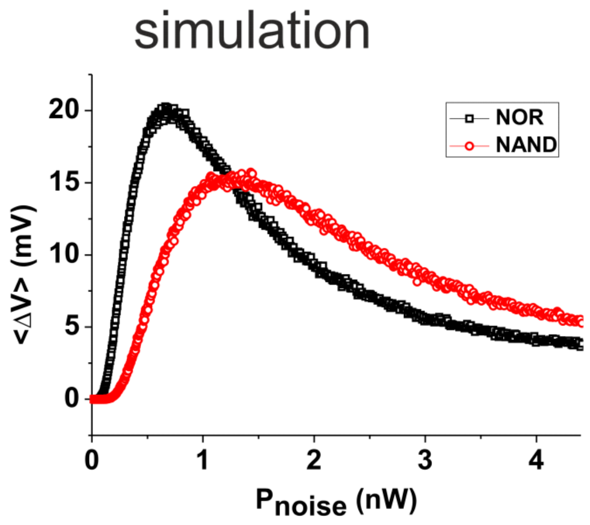
- Universal logic gate switching solely controlled by the noise floor.

- Two universal logic gates: NOR/NAND.

- Switching between the gates only as a function of noise power.

Reconfigurable logic universal gates: Logic stochastic resonance





For the logic NOR gate:

- The mean value difference is defined as

$$<V>=V(I=0)-V(I=1)$$

P_{noise}=0.9 nW the maximum corresponds to the logic NOR

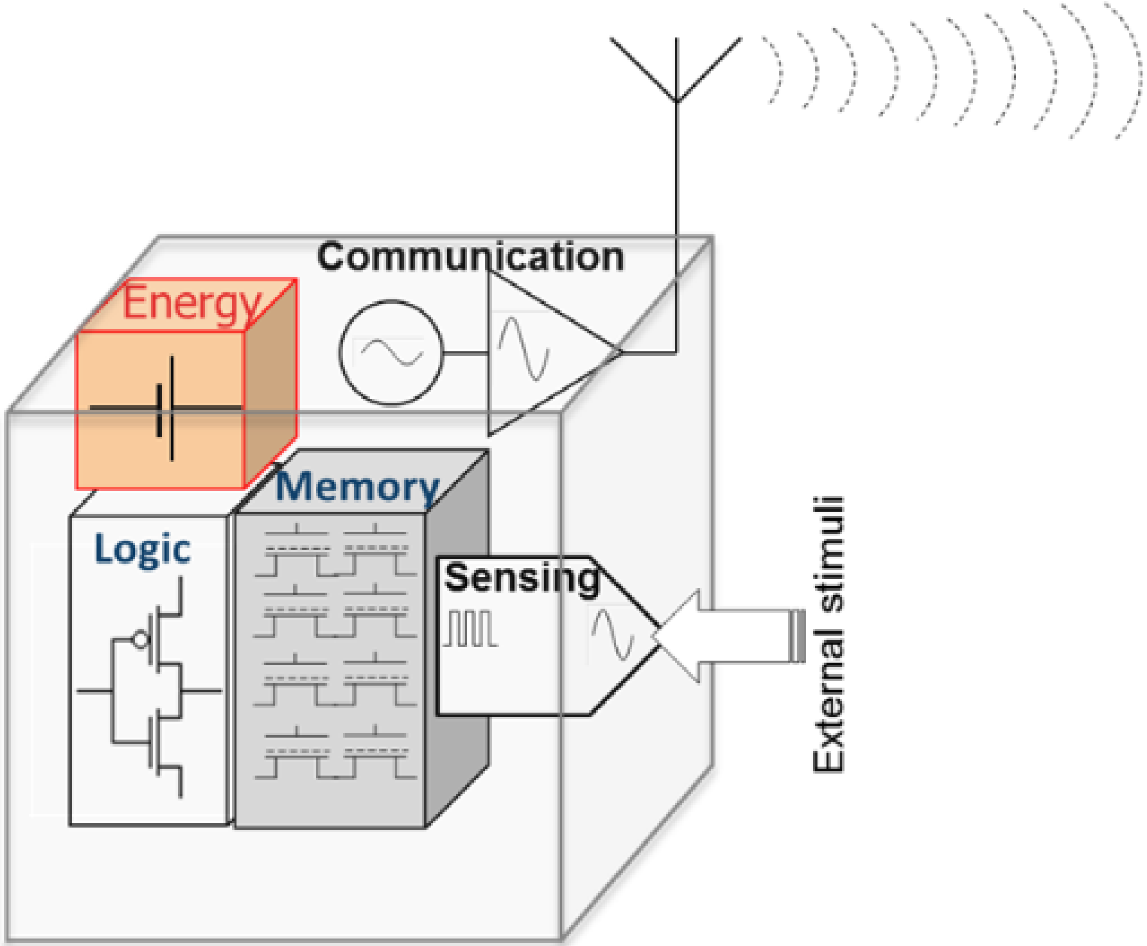
For the logic NAND gate:

- The mean value difference is defined as

$$<V>=V(I=1)-V(I=2)$$

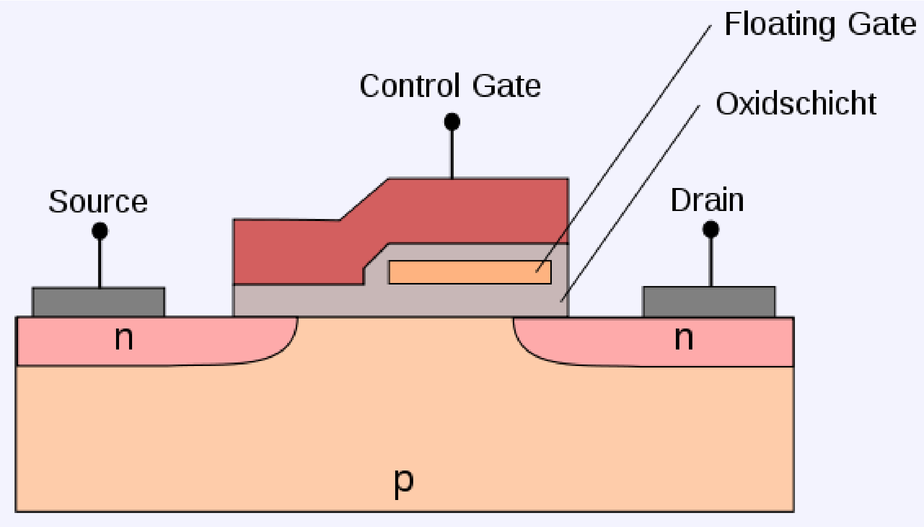
P_{noise} = 1.4 nW the maximum corresponds to the logic NAND

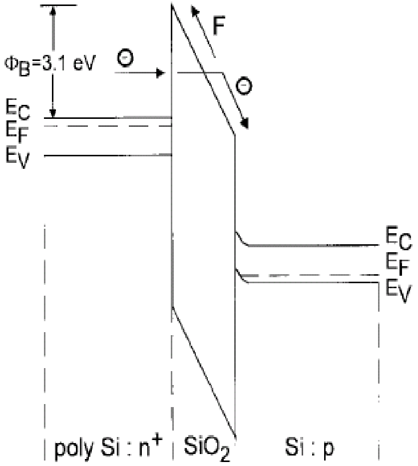
Outline

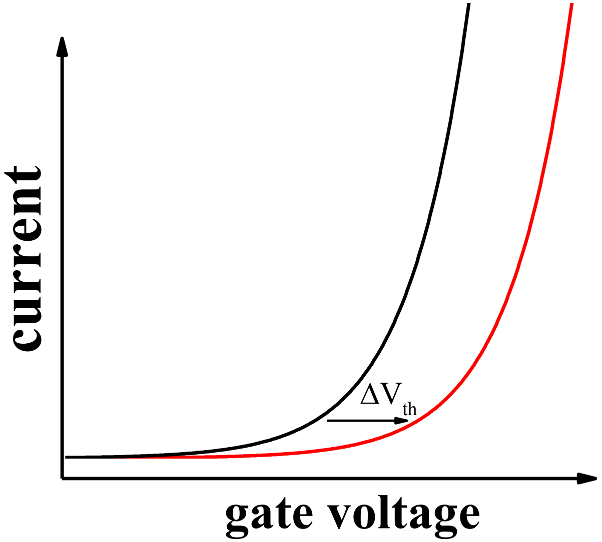


2) The memory part: Quantum dot floating gate transistor

Floating gate transistor: Short introduction







Floating gate transistor:

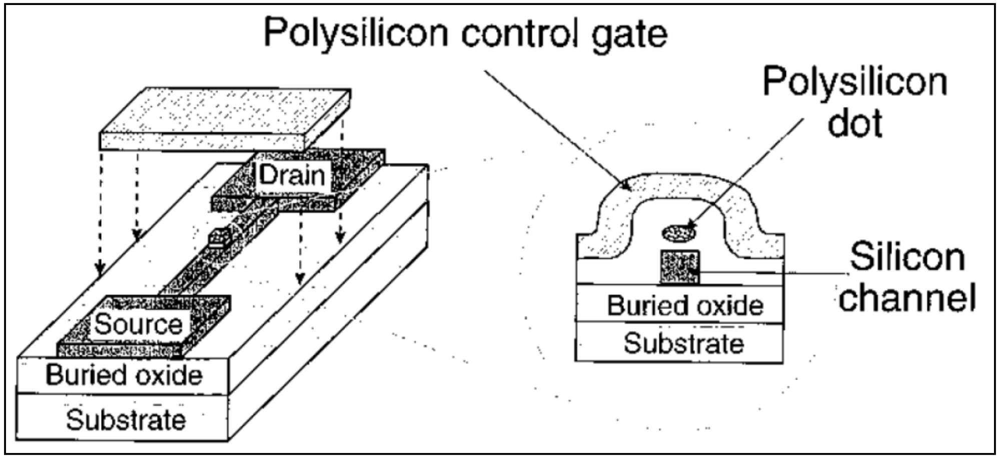
- Non-volatile memory having a retention time of more than 10 years.
- A floating gate in a metal-oxide semiconductor field effect transistor (MOSFET) acts as the storage unit.
- SiO_2 barriers with an energetic height of 3.2 eV.

Threshold voltage shift:

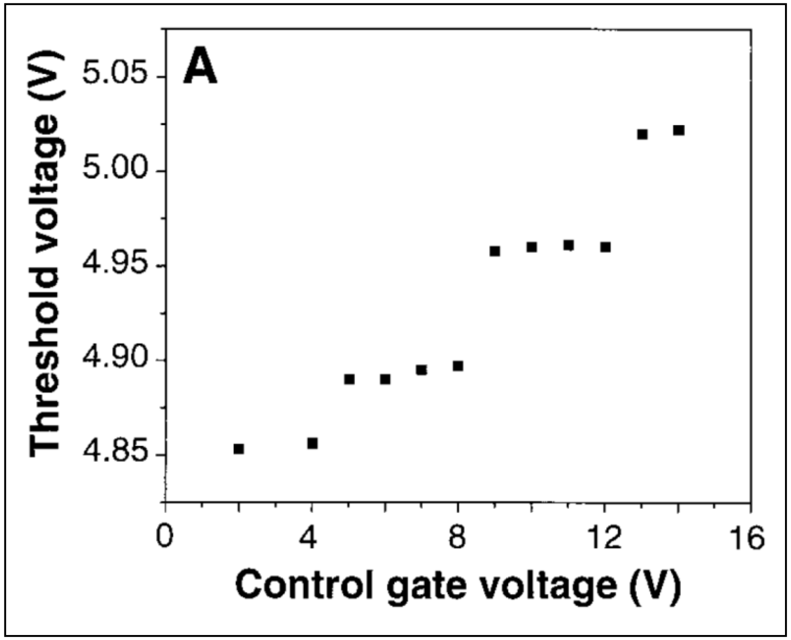
$$\rightarrow \quad \Delta V_{th} = \frac{\Delta Q}{C_{eff}}$$

QD floating gate transistor: a quantum dot-based memory device

Demonstration of working principle of a ‘silicon single-electron memory transistor‘.



L. Guo et al., Science 275, 649 (1997)



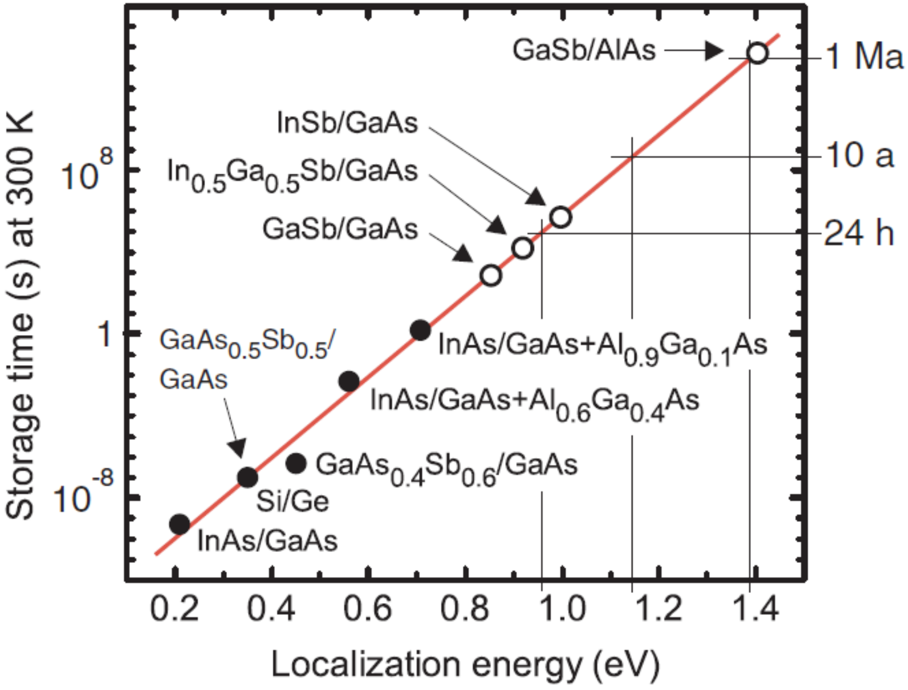
Discrete shift of threshold voltage in dependence on the number of stored electrons on the dot with

$$V_{th,up} = \frac{ne}{C_{dg}}$$

QD floating gate transistor: a quantum dot-based memory device

Advantages compared to Si/SiO$_2$ system:

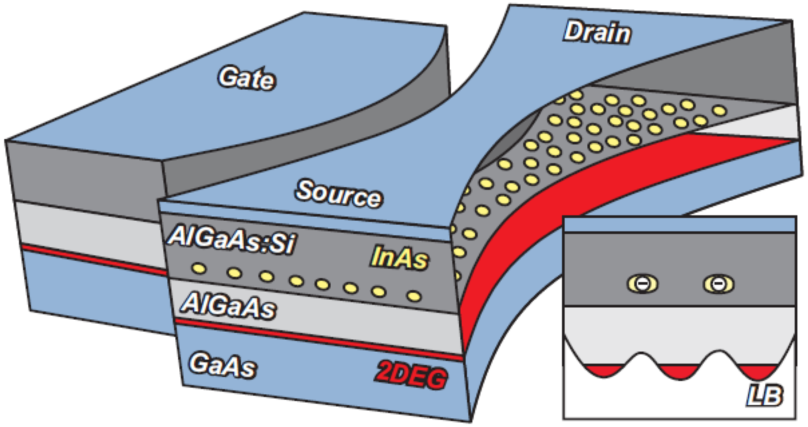
- The height of the barrier can be designed.
- Defect-free interfaces.
- Writing or erasing the device does not damage the structure.
- Hole-based charge storage can be used.



A. Marent et al., Semicond. Sci. Technol. **26** (2011) 014026

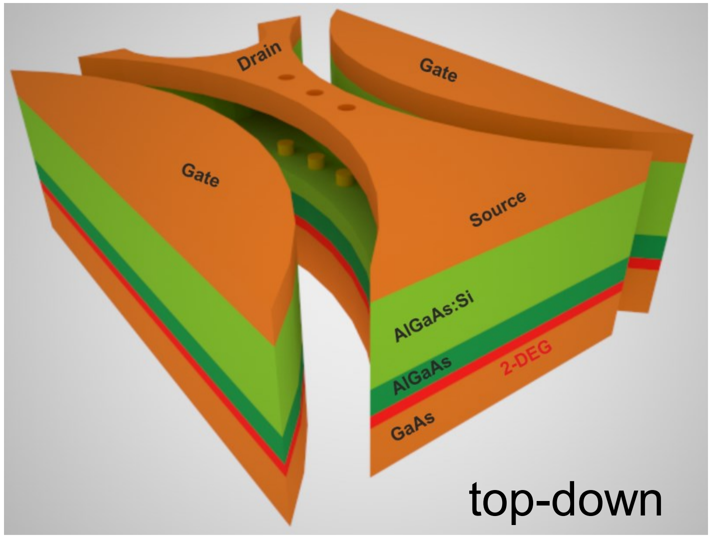
QD floating gate transistor: a quantum dot-based memory device

QD-Flash memory with self-assembled QDs:



bottom-up

QD-Flash memory with positioned site-controlled QDs:

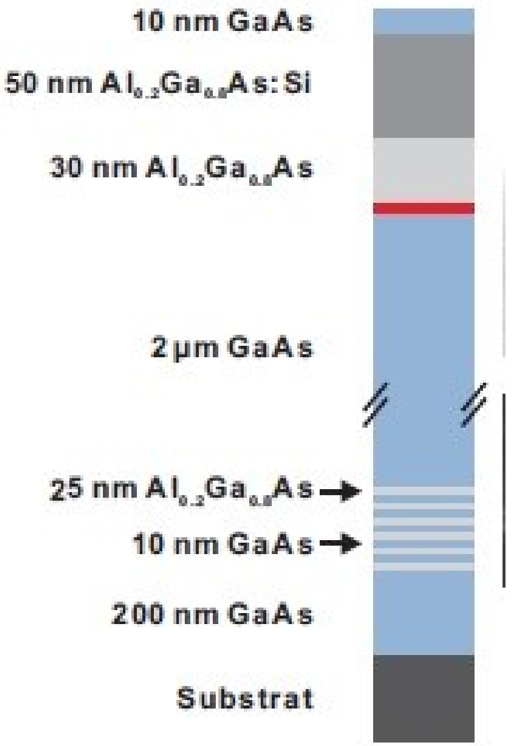


top-down

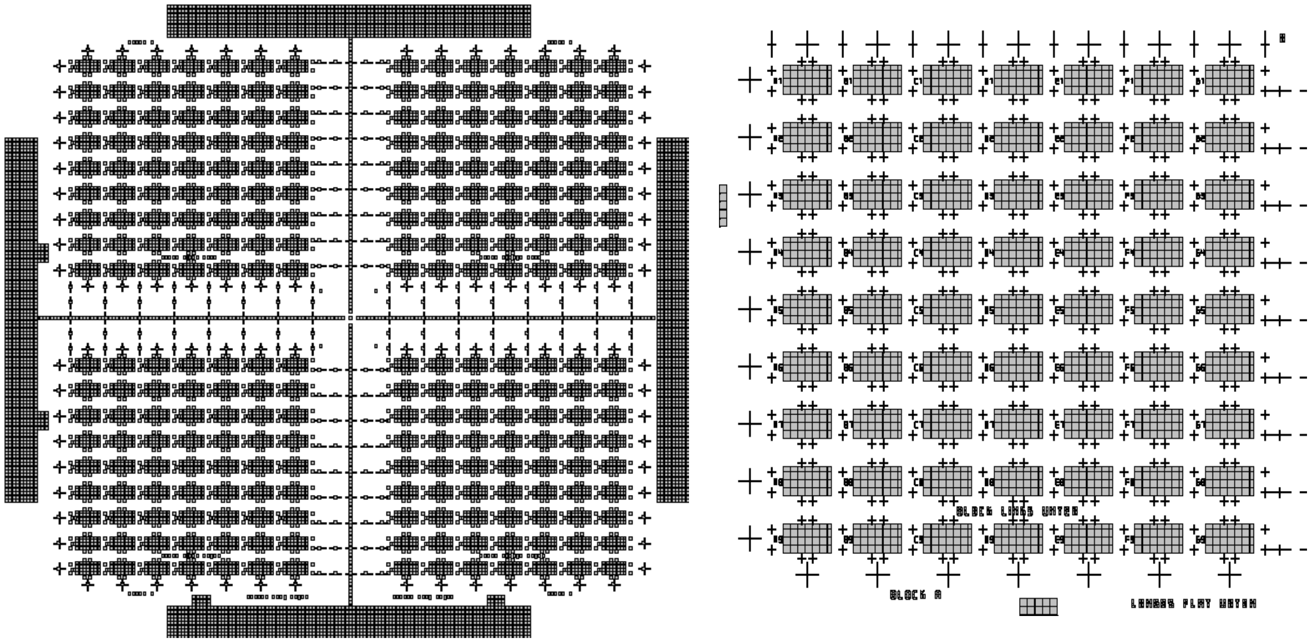
- Self-assembled QDs are randomly distributed.
- Charging of several QDs contribute to the threshold voltage shift.
- Ensembles of QDs are typically not practical for the study of single electron properties.

→ **Control the number and position of the QDs.**

Fabrication of QD memories with positioned and site-controlled quantum dots



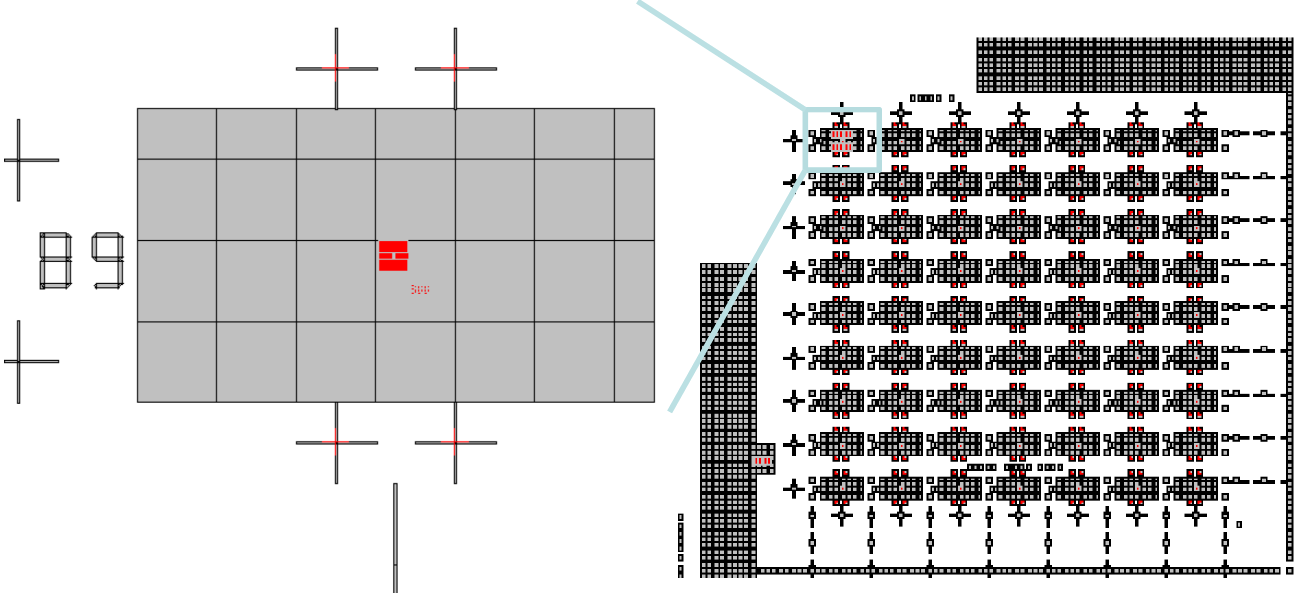
Pictures from our e-beam lithography system



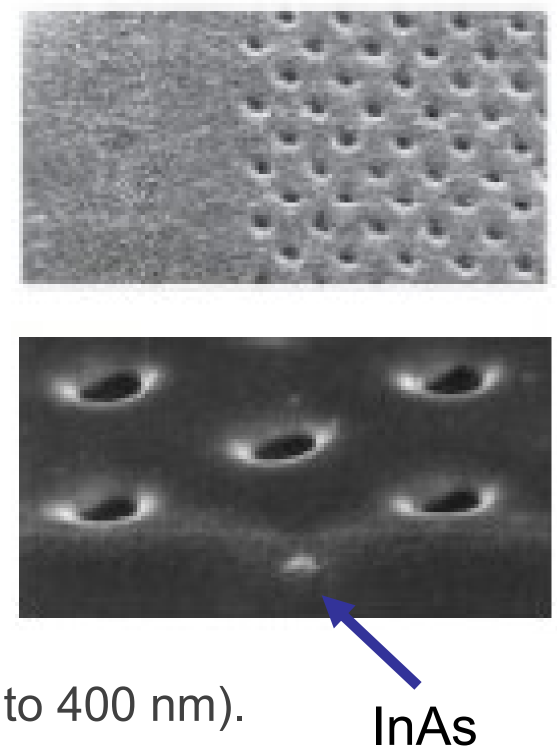
Level 1-Growth:
Growth of high mobility 2DEGs on the basis of AlGaAs/GaAs.

Level 2-Mesa definition:
Optical lithography and wet chemical etching of mesas with a depth of 500 nm – 1000 nm.-> **4** blocks with **63** possible structures

Fabrication of QD memories with positioned and site-controlled quantum dots



Electron microscopy images



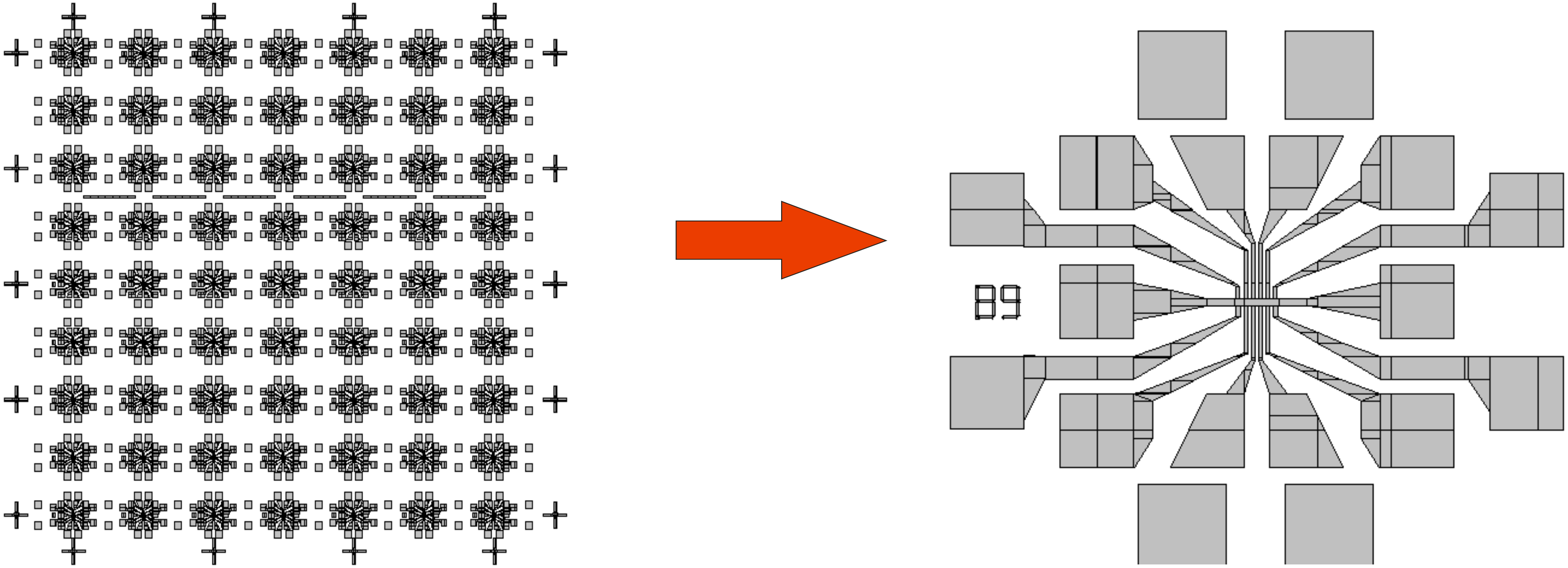
Level 3 – Nanoholes:

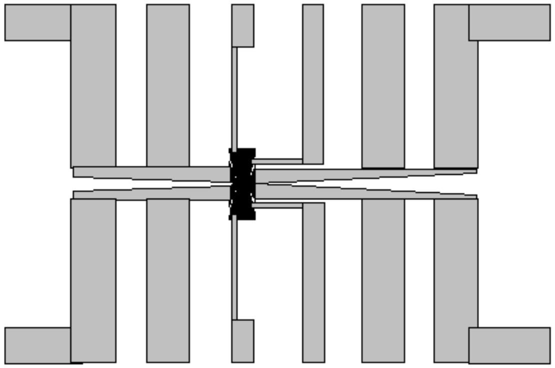
1) 100 nm PMMA. 2) E-beam lithography (periods from 200 to 400 nm).
3) Develop the resists. 4) Dry chemical etching.

Level 4 - Overgrowth process:

Overgrowth process with InAs and GaAs

Fabrication of QD memories with positioned and site-controlled quantum dots





Level 5 – Hallbars:

Optical lithography and wet chemical etching.

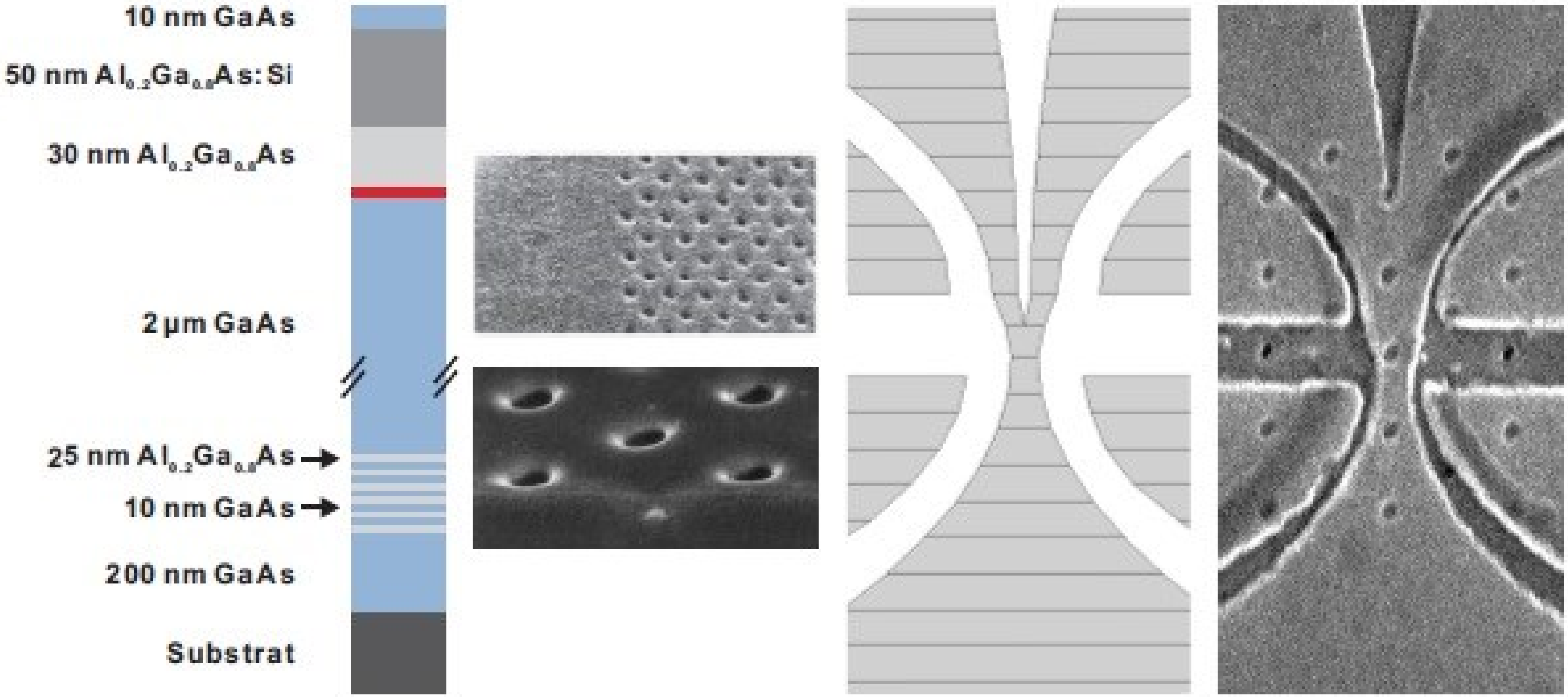
Level 6 – Contacts:

Evaporate the contacts (AuGe/Ni/Au)

Fabrication of QD memories with positioned and site-controlled quantum dots

Level 7 - Y-branch:

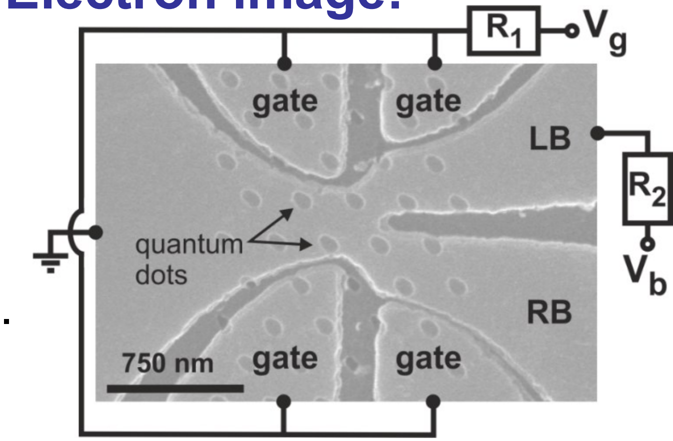
E-beam lithography and dry chemical etching

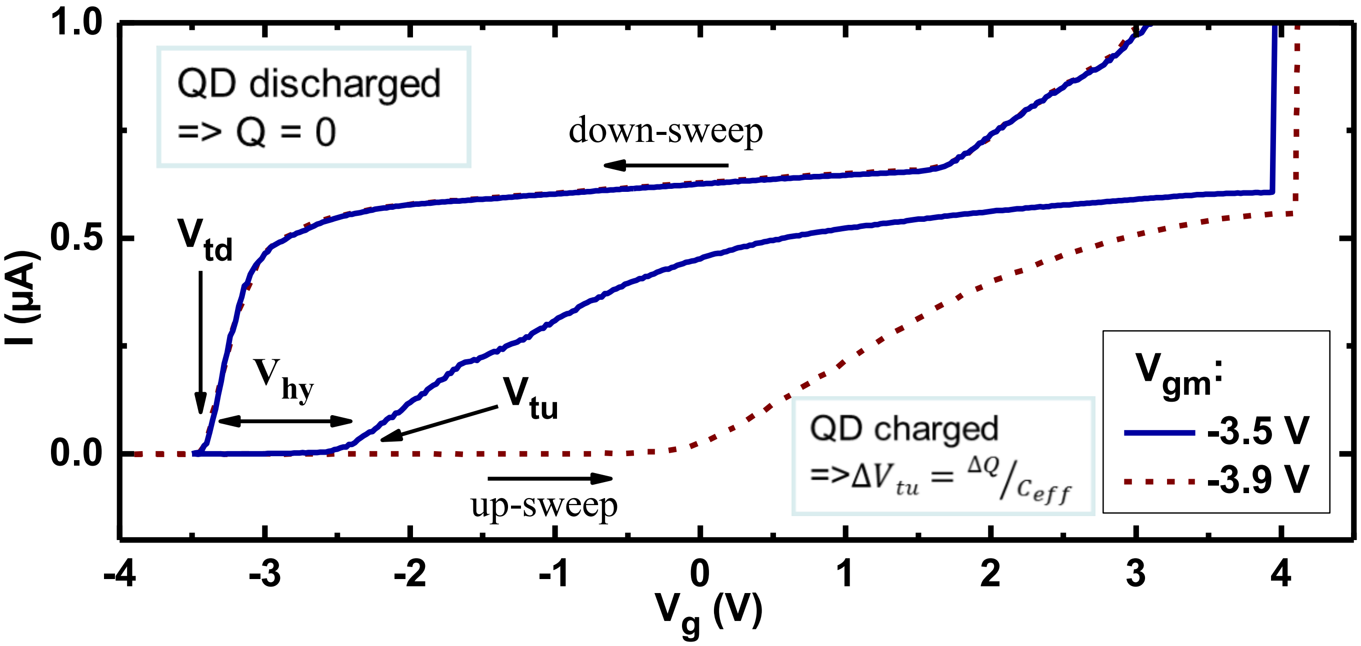


Floating gate transistor – variation of charging voltage

- I(V_g)-characteristics for two charging voltages.
- Trace during down-sweep remains unaltered.
- V_{tu} shifts towards larger values when decreasing V_{gm}.

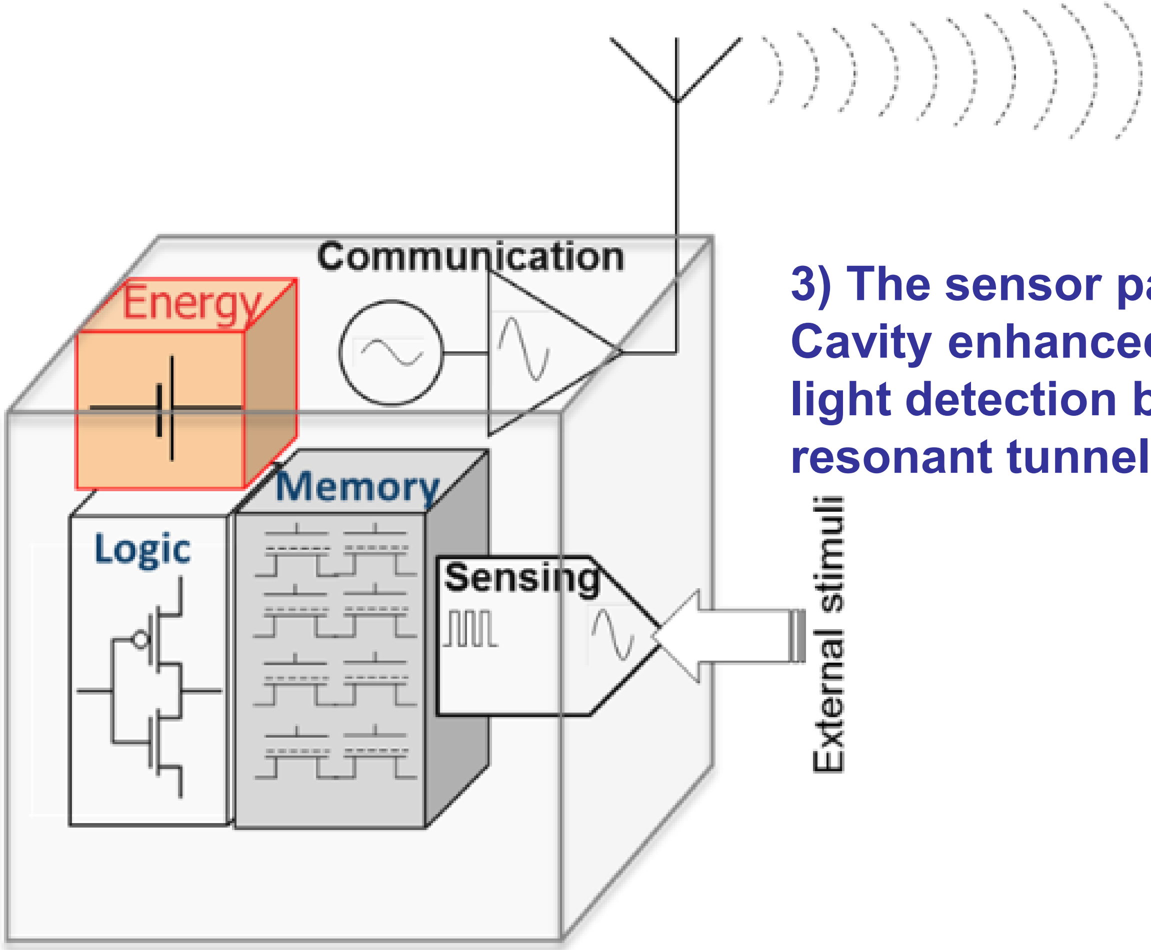
Electron image:





$$V_{hy} = V_{tu} - V_{td}$$

Outline



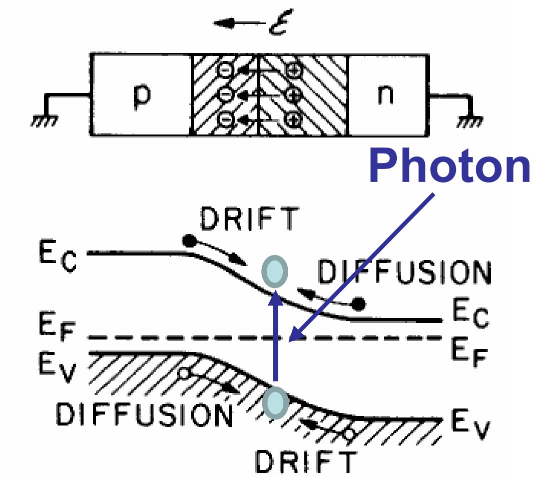
3) The sensor part: Cavity enhanced light detection by resonant tunneling

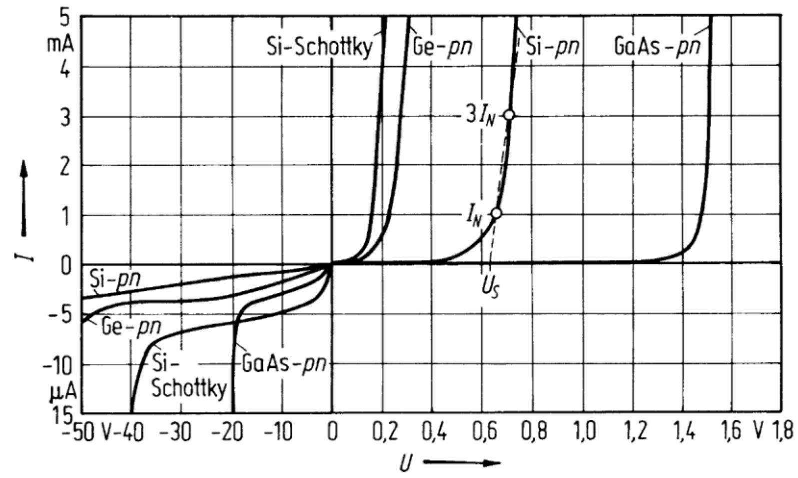
Pin-photodiodes: Light detection at telecommunication wavelengths

Photocurrent:

$$\Delta I = \eta \cdot SE \cdot M \cdot P$$

$$SE = \frac{e\lambda}{hc}$$



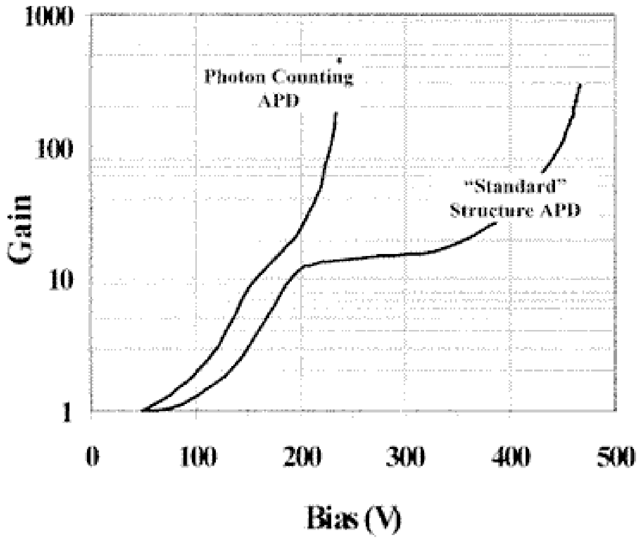


Sensitivity:

$$S = \frac{\partial \Delta I(V,\lambda)}{\partial P}$$

InGaAs: APD ~ 10 A/W

Gain = 10



But, noise:

$$i_{APD} \propto M, I_{dark}$$

P = *light power*; M = *gain*

SE = *spectral response*

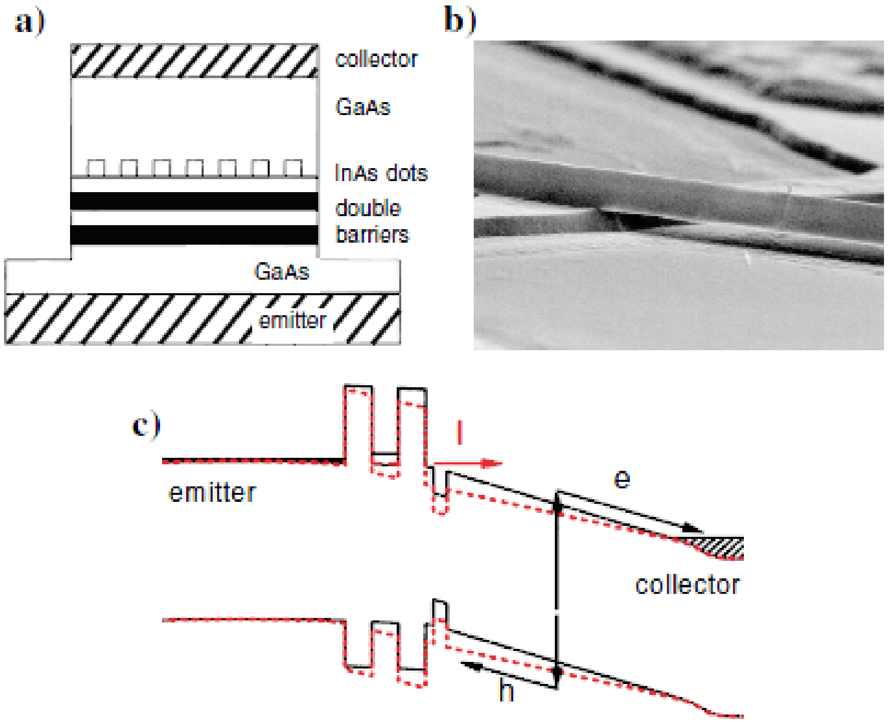
η = *Quantum efficiency*

Light detection in RTDs with embedded quantum dots

RTD light detection with embedded quantum dots:

- GaAs or InGaAs based RTDs with InAs quantum dots.
- Single-photon detection for light in the visible and IR wavelength region at ~ 4K.

J. C. Blakesley, et al. ,PRL **94,** 067401 (2005)



Pros:

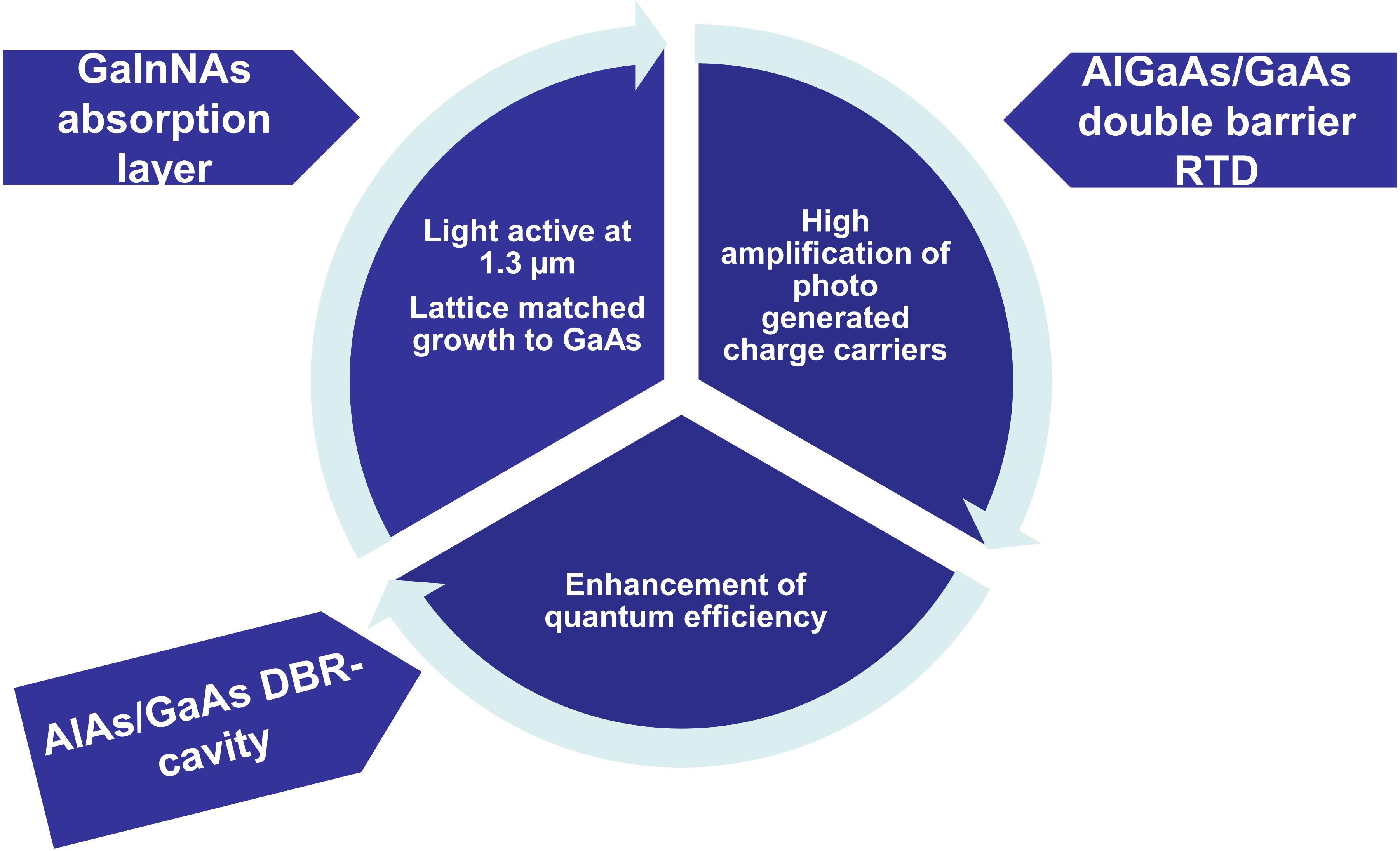
- It works!!
- Single photon resolution even for IR.

Cons:

- InP wafer for 1.3 µm -> expensive.
- Cryogenic temperatures.

→ Light sensing with RTDs at telecommunication wavelengths: **1.31** and **1.55 µm.**

Light detection in RTDs: Our approach



GaInNAs absorption layer

Light active at 1.3 µm

Lattice matched growth to GaAs

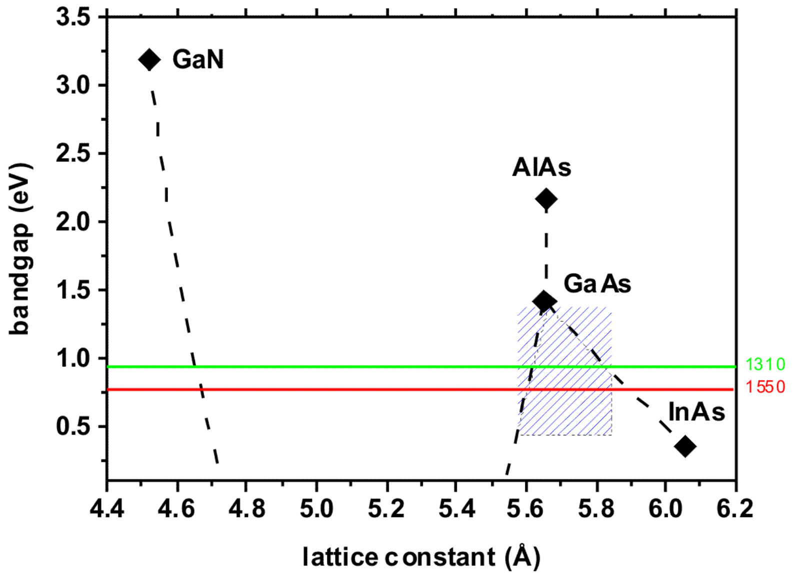
AlGaAs/GaAs double barrier RTD

High amplification of photo generated charge carriers

Enhancement of quantum efficiency

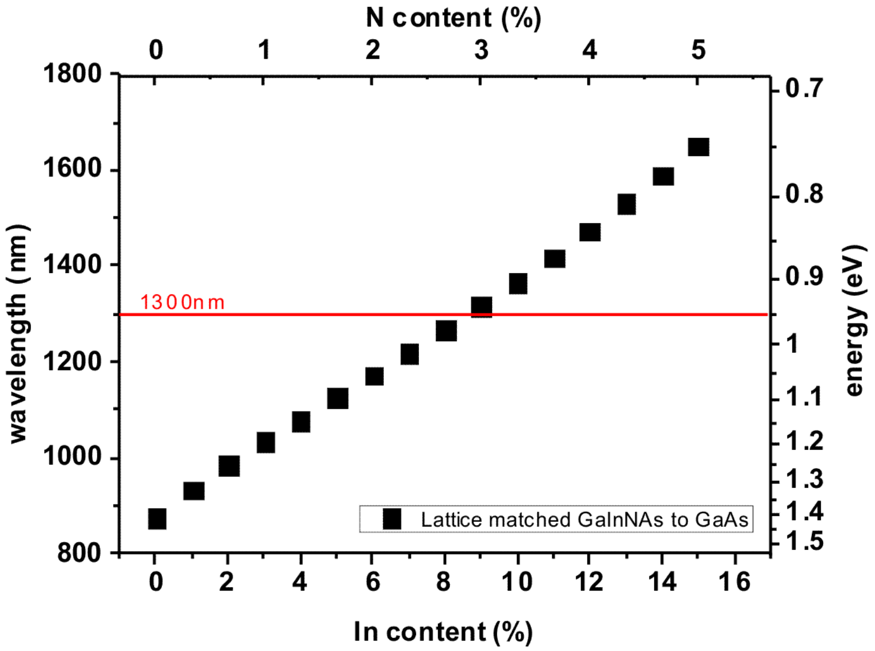
AlAs/GaAs DBR-cavity

The quaternary GaInNAs: Band gap engineering and lattice matched growth to GaAs



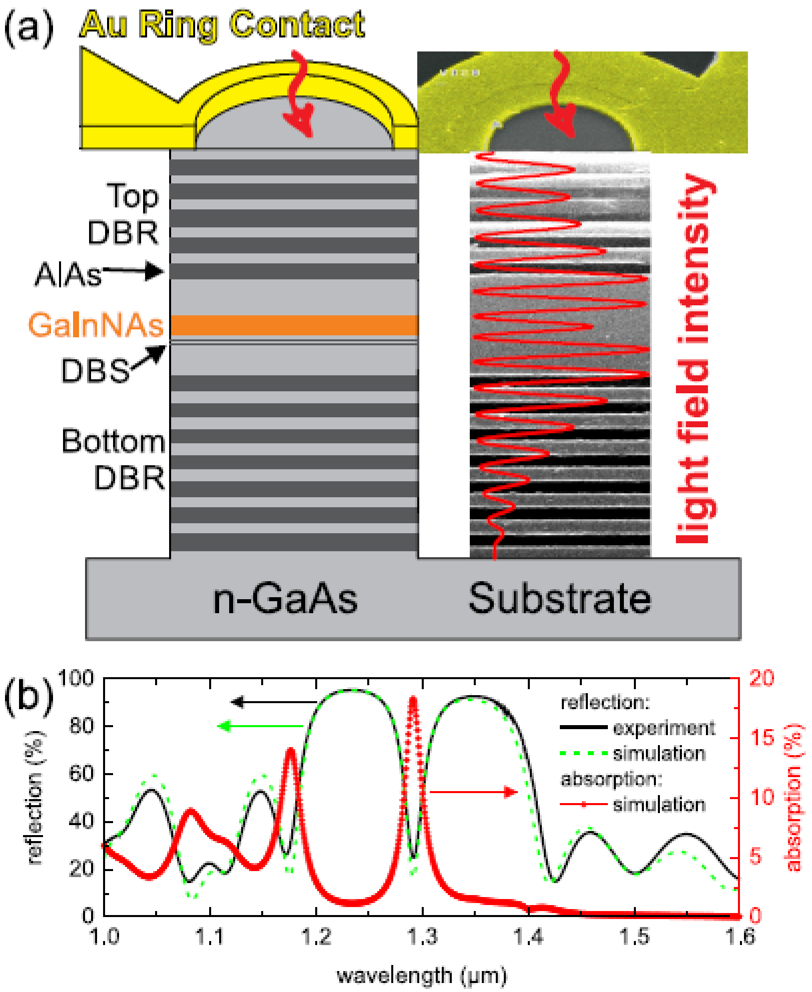
- Dashed lines correspond to the ternary materials e.g. InGaAs
- Blue shaded: Realizable area of GaInNAs

- Band gap energy of GaInNAs depends on the In and N contents.
- For lattice matched growth on GaAs:
  In[%]/N[%] ~ 3
- For 1.3 µm:
  $\mathbf{Ga_{0.91}In_{0.09}N_{0.03}As_{0.97}}$



Kudrawiec *et al.*, J. Appl. Phys. 101, 023522 (2007).

Cavity enhanced light detection by resonant tunneling at telecommunication wavelengths



A. Pfenning et al., Appl. Phys. Lett. 104, 101109 (2014)

Sample Design:

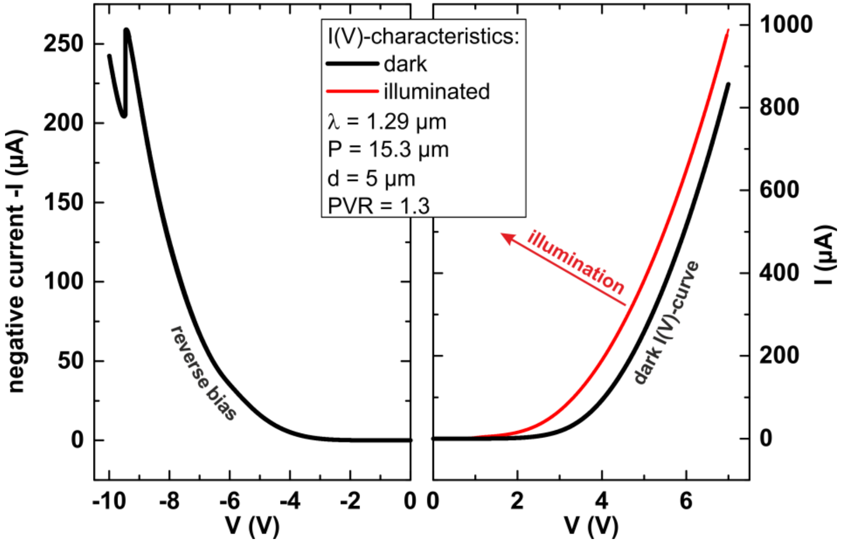
- Cavity consists of ***5/7* GaAs/AlAs DBR mirror pairs**, with **width of 2*λ*** .

DBR-Properties:

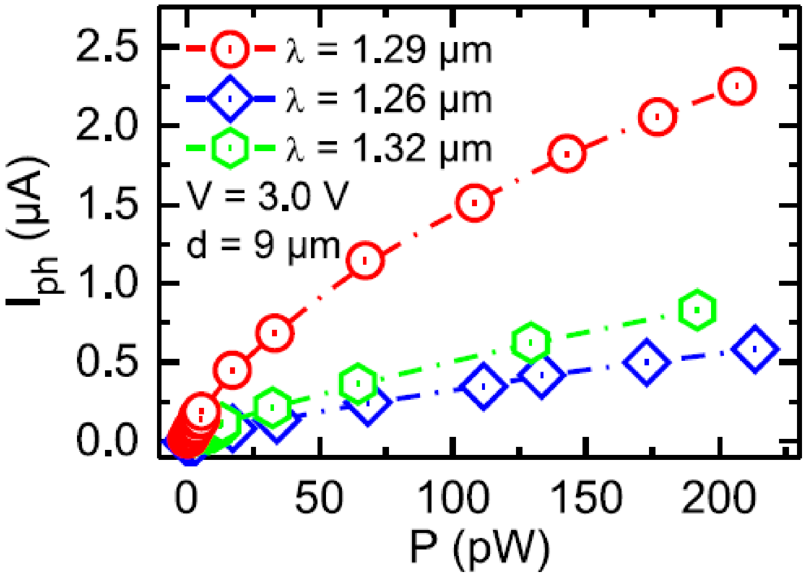
- Resonance *λ* **= *1.29 µm***
- Quality factor ***Q*** = ***50***

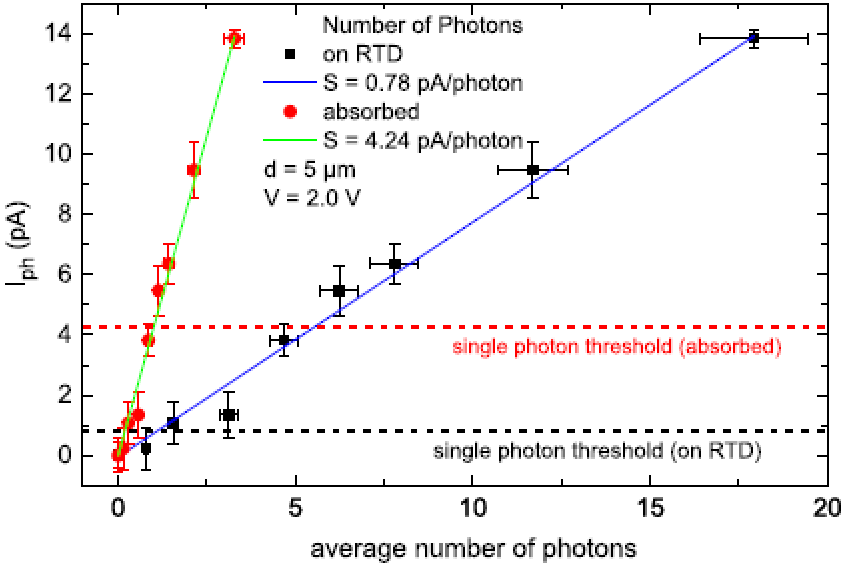
Electrical-Properties:

- Peak-to-Valley Ratio ***PVR = 1.3***
- I(V)-shift under illumination
- No hole accumulation for reverse bias



Cavity enhanced light detection by resonant tunneling at telecommunication wavelengths





CW-Measurements:

- Small signal linear fit:

  S*(*1.29 μm*) = *31.2 kA W⁻¹
  S*(*1.26 μm*) = *2.90 kA W⁻¹
  S*(*1.32 μm*) = *5.89 kA W⁻¹

- Enhancement of a factor ***11*** and ***5!***

Pulsed Excitation:

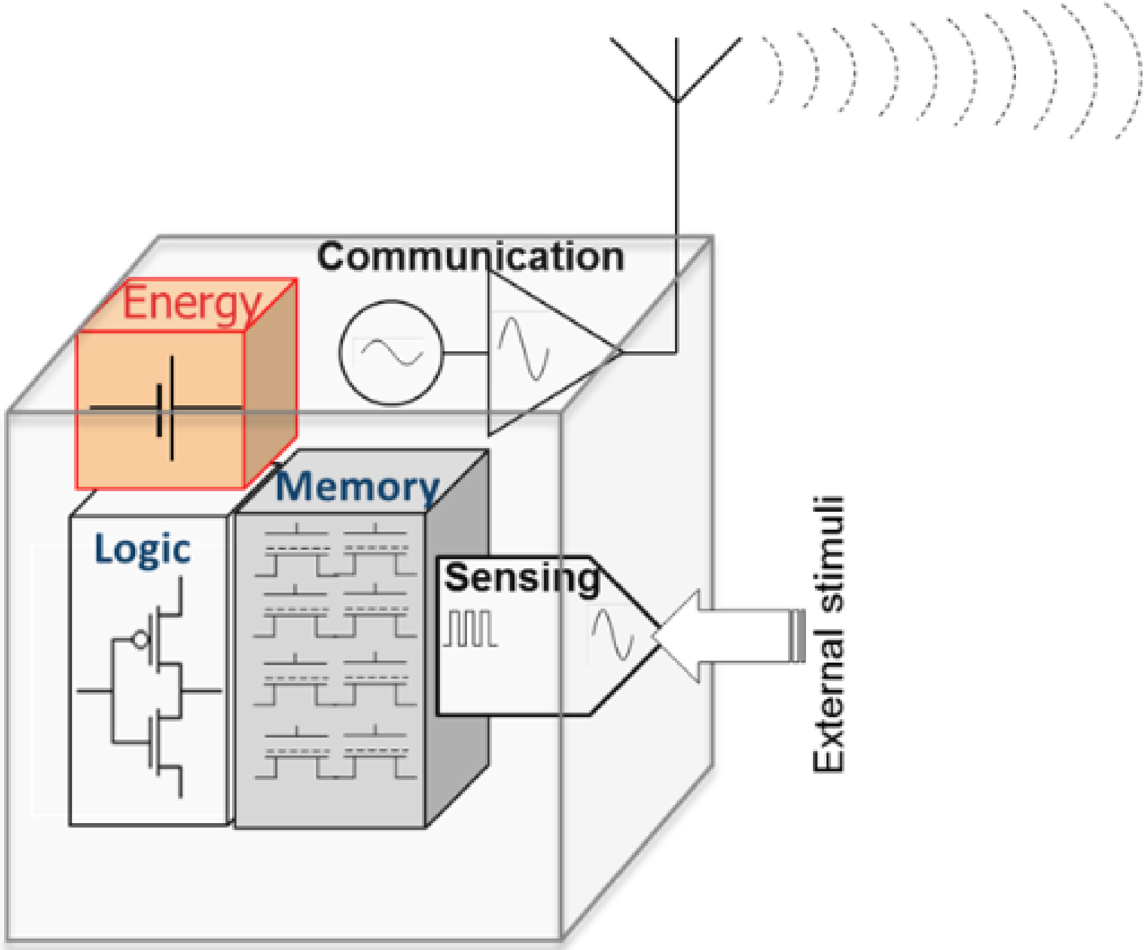
- For a single photon:

  $$I_{ph} = (779 \pm 15)\ \mathrm{fA\ photon}^{-1}$$

- ***Single Photon Detection possible!***

Outline

4) The energy source part: Voltage fluctuation to current conversion



Energy harvesting in nanoelectronic devices: Optimal energy quanta to current conversion

Theory developed by:

- Rafael Sánchez, and Markus Büttiker: “Optimal energy quanta to current conversion.” Phys. Rev. B 104, 076801 (2011).
- Björn Sothmann, Rafael Sánchez, Andrew N. Jordan and Markus Büttiker “Rectification of thermal fluctuations in a chaotic cavity heat engine.” Phys. Rev. B 85, 205301 (2012).

Sánchez et al.

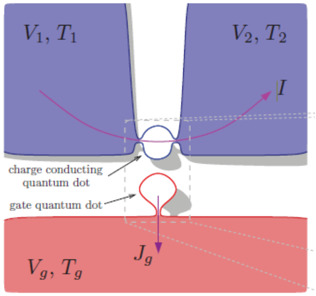
Coulomb blockade regime:

Quanta relation:

$$\frac{I}{q} = \frac{J_g}{E_C}$$

Efficiency:

$$\eta(V_0) = \eta_c$$



Sothmann et al.

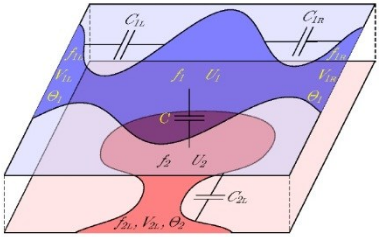
Chaotic cavity regime:

Maximum power:

$$P_{max} = \frac{\Lambda^2}{4G_1\tau_{RC}^2}(k_B(\Theta_1 - \Theta_2))^2$$

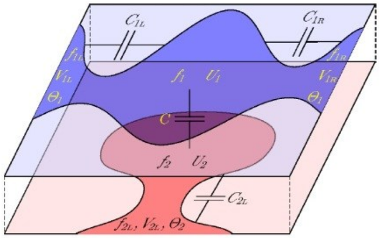
Efficiency:

$$\eta_{\max} @ P_{\max}$$

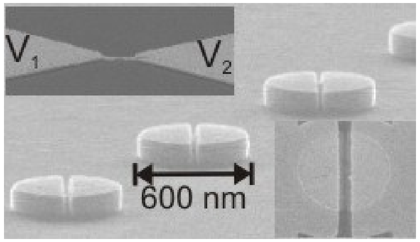


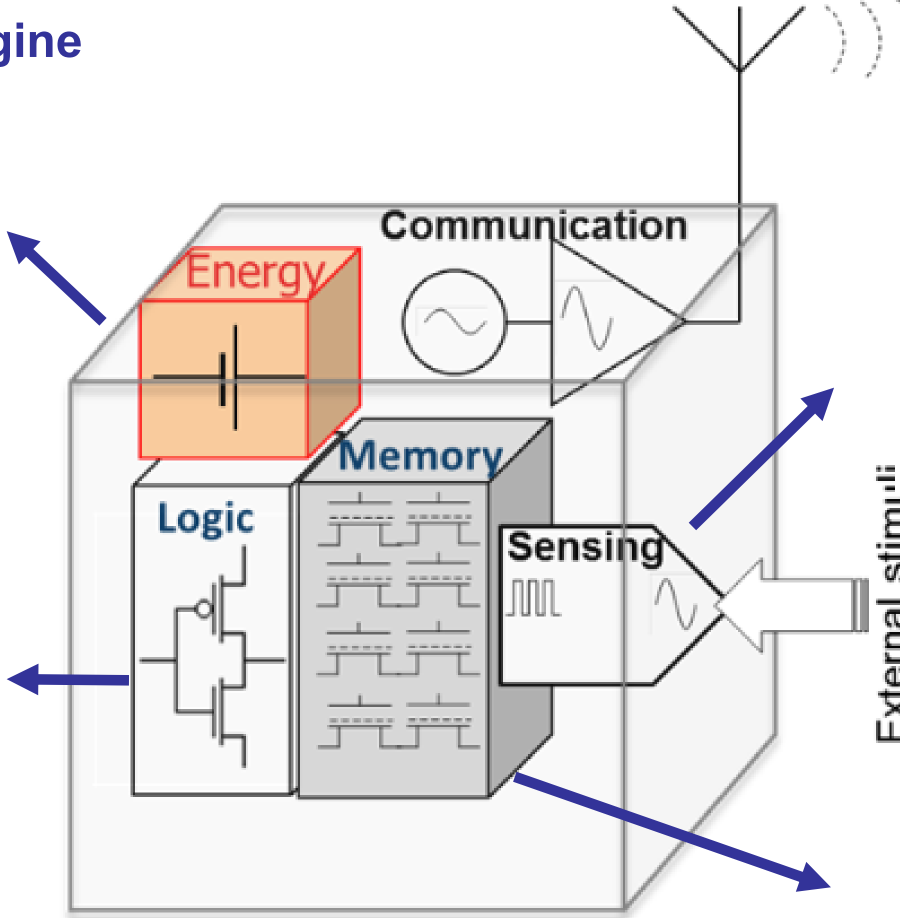
Summary and take home message…

Coupled QD system = Efficient heat engine

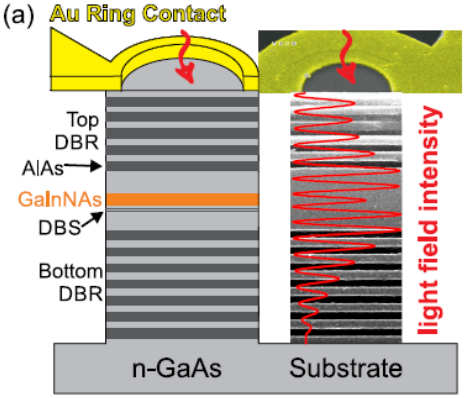


Universal and reconfigurable logic gates





Cavity enhanced light detection by resonant tunneling



QD flash memory